

DB1-1 MULTIFUNCTION LED DISPLAY BOARD

2020.08.08

Lucid Technologies
<http://www.lucidtechnologies.info/>
Email: info@lucidtechnologies.info

Copyright (C) 1999-2020 by Lucid Technologies
All rights reserved

The information in this manual has been carefully checked and is believed to be accurate. However, Lucid Technologies makes no warranty for the use of its products and assumes no responsibility for any errors which may appear in this document. Lucid Technologies reserves the right to make changes in the products contained in this manual in order to improve design or performance and to supply the best possible product. Lucid Technologies assumes no liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

CONTENTS

- 1.0 Introduction
- 2.0 Circuit Description
- 3.0 Construction

Appendix A Parts List

Appendix B Parts Placement

Appendix C Hardware Specifications

Appendix D Schematics

Appendix E MC14489 datasheet

1.0 Introduction

The DB1 multi-function LED display board is available in two models - the DB1-CLOCK and the DB1-NUMERIC. The only difference in the construction of the two models is the LED display module soldered to the board.

The DB1 is compatible with the Motorola SPI and National MICROWIRE serial interfaces. A software "bit-banging" interface can easily be written for any microcontroller that doesn't have one of these synchronous serial ports. Power and serial data come to the DB1 via 5-pin connector J1.

The DB1 was designed to fit into the following cases: Simco 150X5, Pactec CM5-125, and Bud 11402. There is ample unused space at the side of the DB1 circuit board for mounting holes to be drilled in other applications.

2.0 Circuit Description

The DB1 is based on the MC14489 integrated circuit, U1. See Appendix E for the MC14489 datasheet. Motorola (now Freescale) calls this chip a "Multi-Character LED Display/Lamp Driver". It's quite a versatile device, capable of driving a 5-digit common-cathode display plus decimal-points, or 25 discrete LEDs, or just about any combination in between. In the DB1 circuit, it drives four 7-segment digits plus colon, or decimal points, while the fifth digit is used to drive the annunciator LEDs. It does this by multiplexing segments a thru h among the five digits, or five banks as they are called on the IC's data sheet. The MC14489's internal oscillator guarantees a minimum refresh rate of 700 Hz, more than fast enough to insure a flicker-free display. Other than the LED display, the only external component required by the MC14489 is a single resistor (R1) to set the maximum segment drive current. Drive currents can go as high as 30 mA per segment but thermal considerations become critical at high drive currents. The DB1 is designed for a peak segment drive current of approximately 12 mA.

Note that the typical applications shown in the MC14489 data sheet have digit-5 as the most

DB1 Display Board

significant digit (54321). However the data sheet for the LED modules used on the DB1 shows digit-1 as the most significant digit (1234). Therefore the DB1 was designed with digit-1 as the most significant digit, be aware of this if you are writing your own driver software for the DB1. MC14489 bank-1 = LED digit-1 = ten's of hours digit, etc.

The MC14489 has an 8-bit configuration register and a 24-bit data register. The configuration register controls blanking and how each digit's data is decoded. There are three possible decode modes; hex, special, and no-decode. The hex and special decode modes are intended for use with 7-segment displays while the no-decode mode is intended for the control of individual LEDs or custom displays. The data register has four bits of data for each of the five digits, three bits to control the activation of the h (decimal point) segment for the various digits, and one bit to set the display to full or half brightness. Communication with the MC14489 is via a synchronous serial interface. For details on programming these registers or the serial interface protocol, consult the MC14489 data sheet which can be downloaded from the Lucid Technologies web site, <http://www.lucidtechnologies.info/>.

2.1 Annunciator LEDs

There are four discrete annunciator LEDs on the DB1. The controlling software can use these as indicators for status, ranges, alarms, etc. For example, a clock could use D2 to indicate AM and D3 to indicate PM. A thermometer could use the annunciator LEDs to indicate Centigrade or Fahrenheit.



3.0 DB1 Construction

You will need the following tools:

- > A low wattage soldering pencil, approximately 15 to 25 Watts.
- > Flux core solder wire, preferably water soluble organic flux.
- > Lead benders.
- > Lead/wire clippers.

Before beginning assembly, check the fit of the board in the card slot of the plastic case. Gently file or sand the sides of the DB1 circuit board until it slides snugly into place. With the DB1 in place, put the top on the case and check that the top and bottom come fully together. If the DB1 is too tall, file or sand the top and bottom of the circuit board until the case closes properly.

DB1 Display Board

3.1 Circuit Board Assembly

Carefully check the DB1 circuit board for shorted or incomplete traces. Check all parts against the list in Appendix A. Check the value/type of each part as you assemble the board. Clip excess lead length from each component after it's soldered.

NOTE: The LED display module and discrete LEDs are inserted from the front of the board and soldered on the back. All other components are inserted from the back of the board and soldered on the front. See the illustrations in Appendix B.

Begin assembly on the back side of the circuit board. Check off each instruction as you proceed.

___ R1	3.3K, 1% (orange-orange-black-brown)
___ R2,R3,R4	10K, 5% (brown-black-orange)
___ C1	0.1ufd
___ U1	MC14489P (note that pin-1 is toward the bottom of the board)
___ J1	5-pin male header. If you are using wires instead of a connector you can attach the wires now or later.

The remainder of the parts insert from the front side.

___ DISPLAY	Insert the display with the decimal points toward the bottom of the board. Solder just one pin on each row of the display then check that the display is flush with the board and level. Reposition the display as required then solder all the pins.
___ D1	Insert the longer lead of the LED through the round pad. Flip the display on its face so the LED drops to the tabletop. This will make the top of the LED even with the front of the display. Be sure the LED is positioned vertically and solder.
___ D2,D3,D4	Same as D1.

APPENDIX A

DB1 PARTS LIST

Quan.	Ref#	Part
1	DB1-1	Circuit board
1	C1	0.1ufd
4	D1-D4	Red T-1 LED
1	R1	3.3K, 0.25W, 1% (orange-orange-black-brown)
3	R2-R4	10K, 0.25W, 5% (brown-black-orange-gold)
1	U1	MC14489P
1	DISP	CC56-21EWA, 4-digit multiplexed clock display module, or CC56-12EWA, 4-digit multiplexed numeric display module

APPENDIX B

DB1 PARTS PLACEMENT

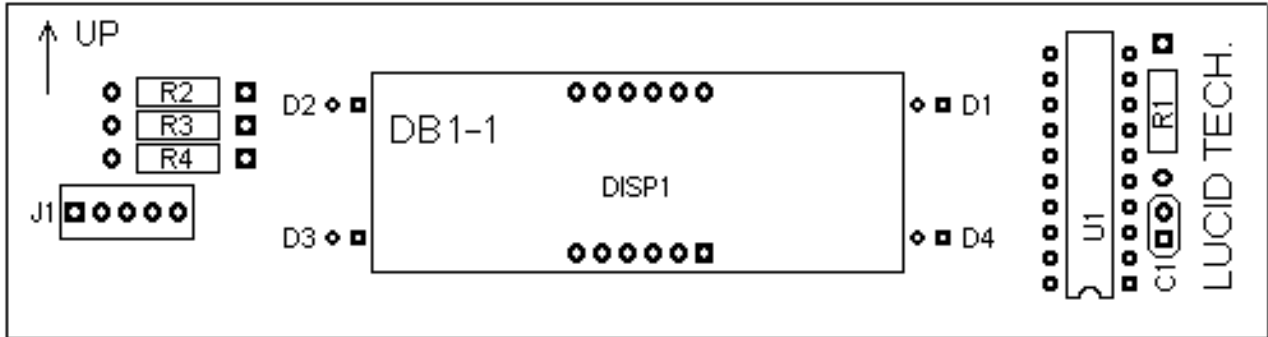


Figure 1 - Rear view of DB1 circuit board.

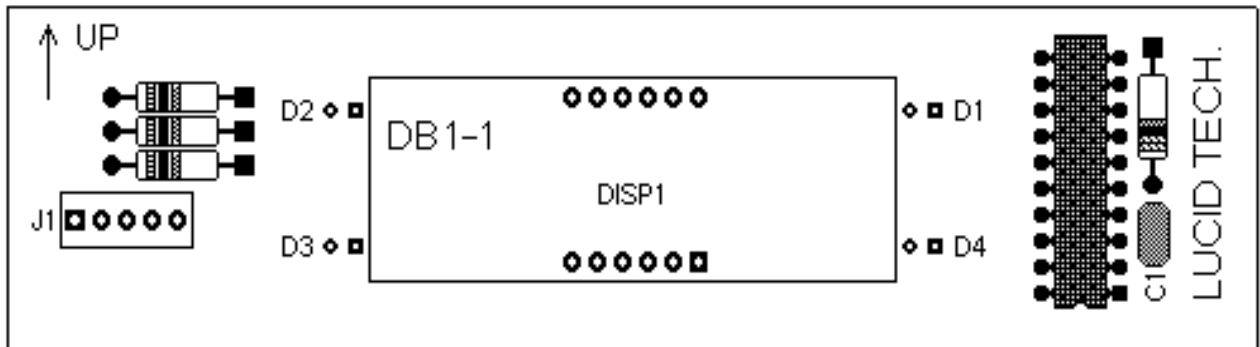


Figure 2 - Rear view of DB1 circuit board with components installed.

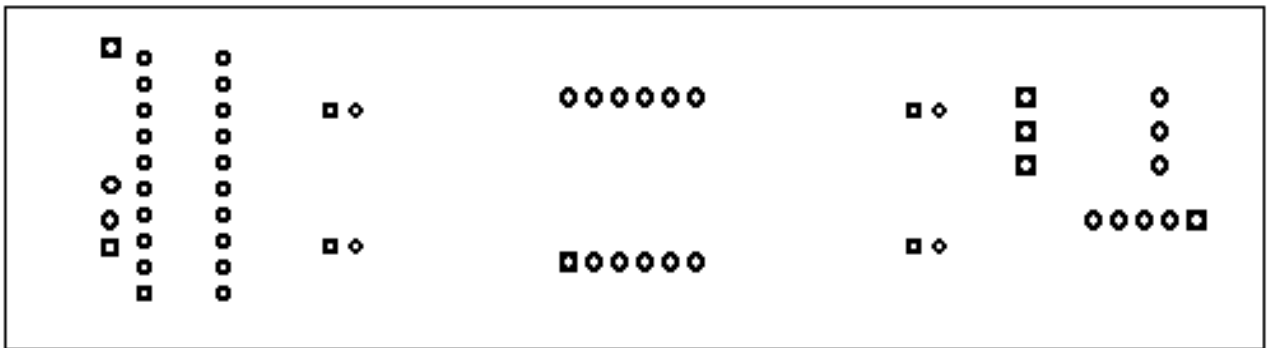


Figure 3 - Front view of DB1 circuit board.

DB1 Display Board

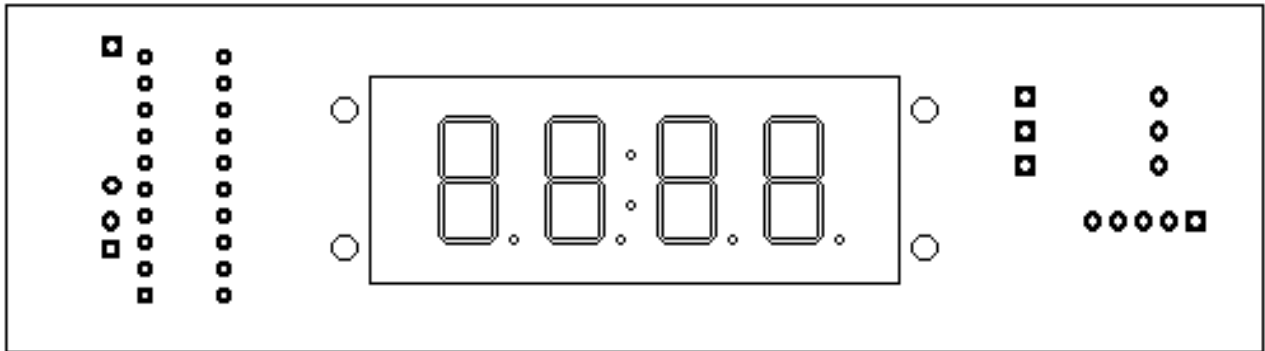


Figure 4 - Front view of DB1 circuit board with display and LEDs in place.

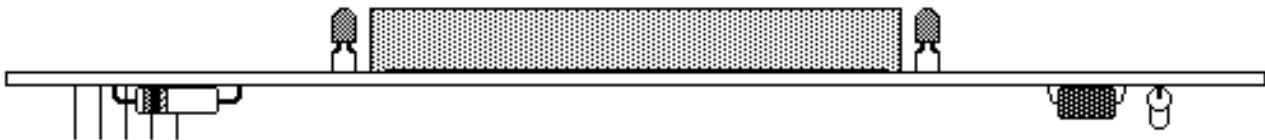


Figure 5 - Top view of assembled DB1 circuit board.

APPENDIX C

HARDWARE SPECIFICATIONS

Circuit board dimensions: 1.26" high by 4.74" wide (32 x 120.4 mm)

Voltage: 5VDC

Current: Approximately 2 mA plus 1.5 mA per active segment or LED

Annunciators:

Four T-1 red LEDs

LED display module:

Dimensions = 0.75" high by 2" wide by 0.315" deep (19 x 51 x 8 mm)

Digit height = 0.56" (14.2 mm)

Color = Red, peak wavelength approximately 627 nanometers

Clock format = Four 7-segment digits with colon

Numeric format = Four 7-segment digits with right-hand decimal points

Connector J1: 5-pin male header

Pin 1 = MC14489 enable, active low

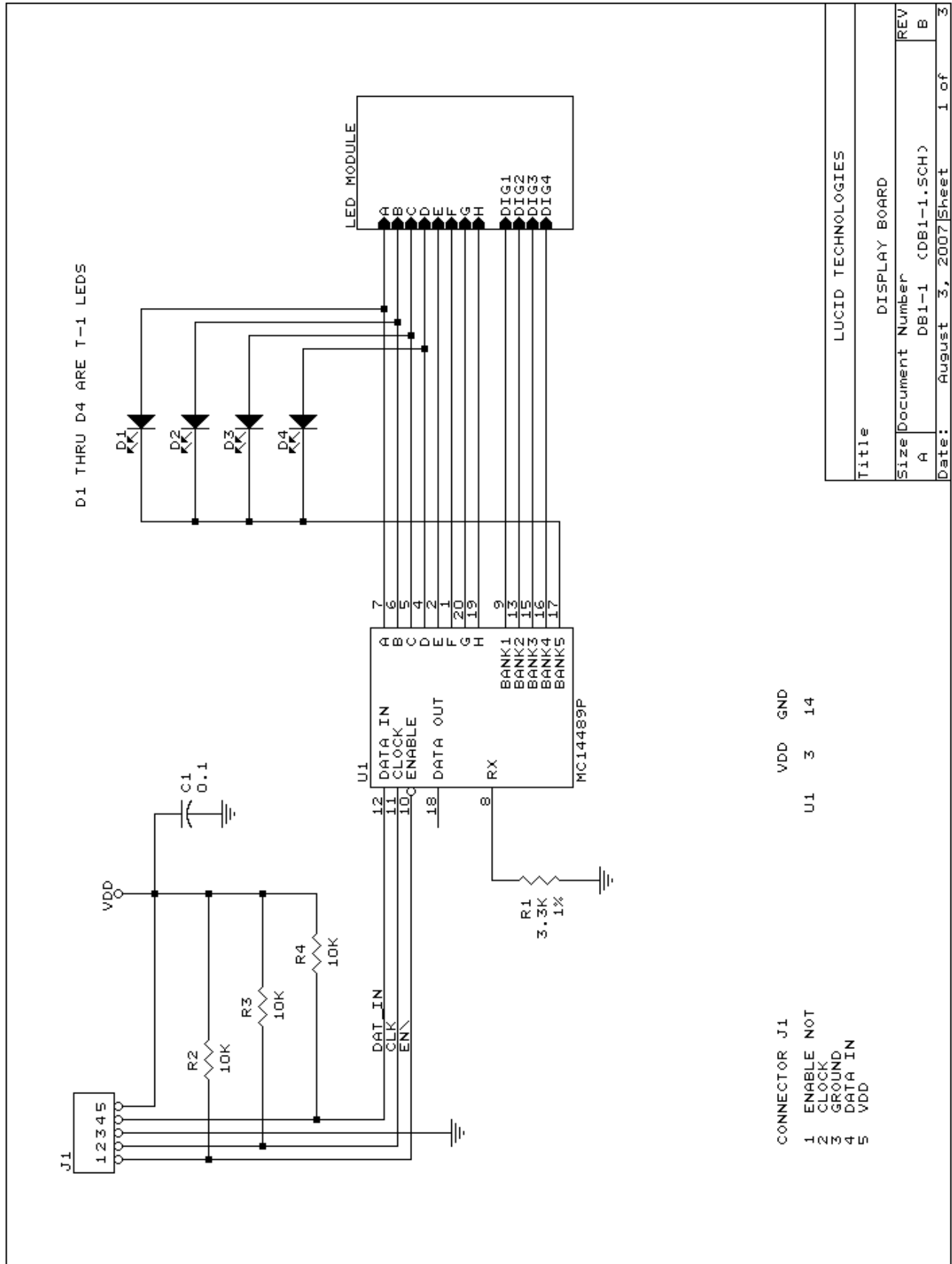
Pin 2 = MC14489 data clock

Pin 3 = Vss, Ground

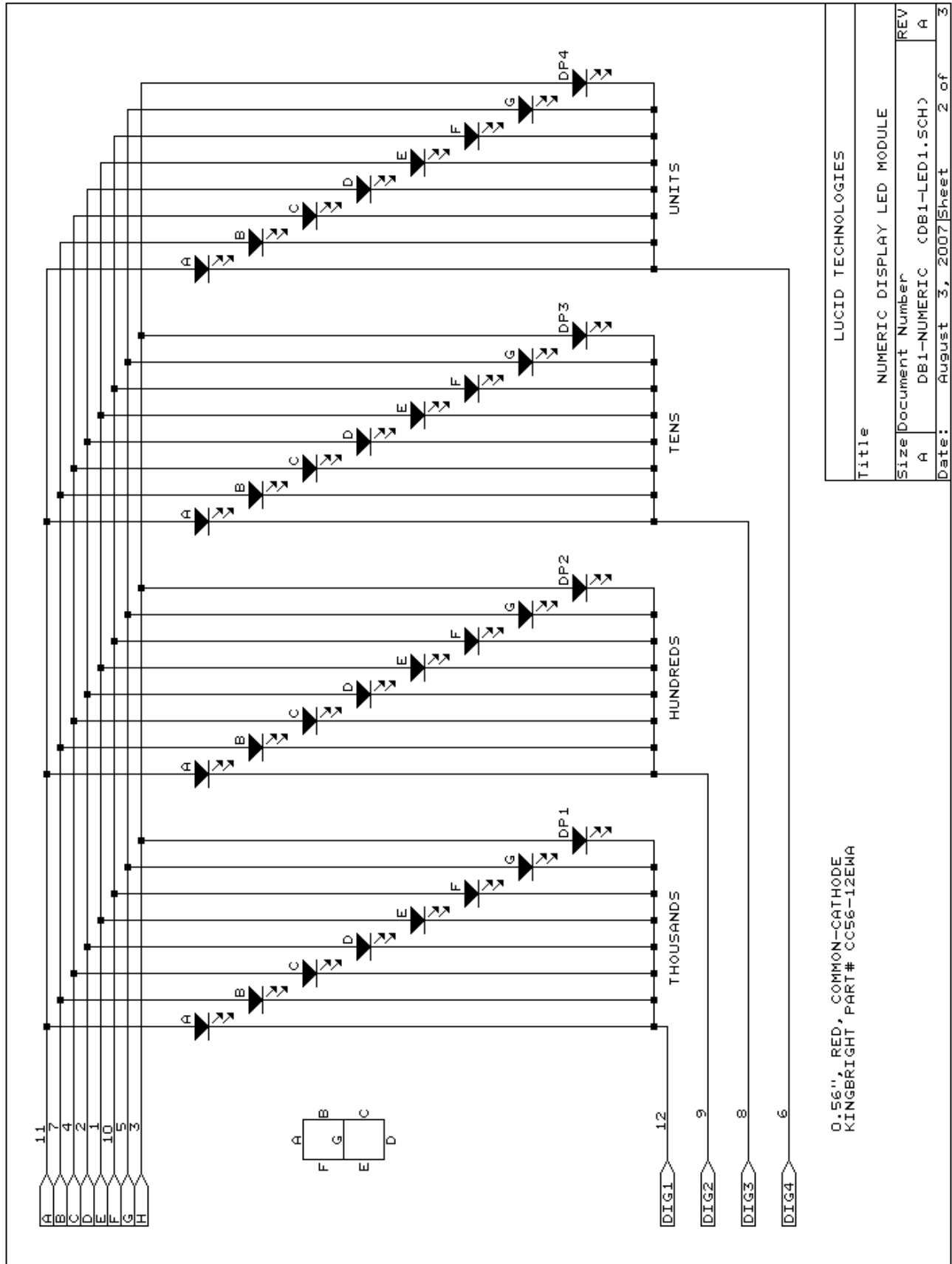
Pin 4 = MC14489 serial data in

Pin 5 = Vdd, 5V

DB1 Display Board



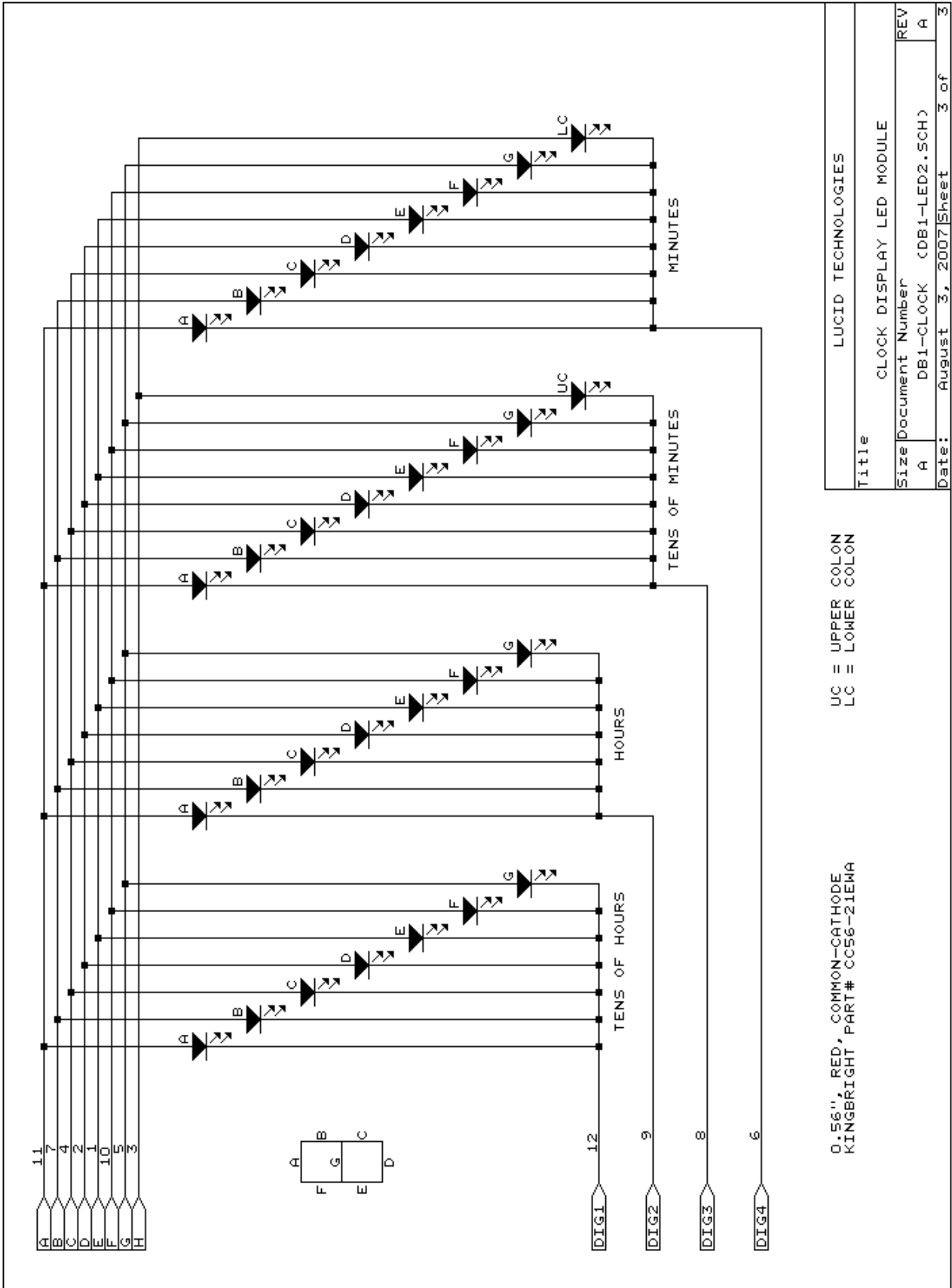
DB1 Display Board



0.56", RED, COMMON-CATHODE
KINGBRIGHT PART # CC56-12EWA

Title		LUCID TECHNOLOGIES	
Size		NUMERIC DISPLAY LED MODULE	
Document Number	REV		
A	DB1-NUMERIC (DB1-LED1.SCH)	A	A
Date:	August 3, 2007	Sheet	2 of 3

DB1 Display Board



DB1 Display Board

Multi-Character LED Display/Lamp Driver CMOS

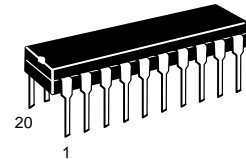
The MC14489 is a flexible light-emitting-diode driver which directly interfaces to individual lamps, 7-segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a multiplexed-by-5 fashion. Communication with an MCU/MPU is established through a synchronous serial port. The MC14489 features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current-setting resistor is the only ancillary component required.

A single device can drive any one of the following: a 5-digit display plus decimals, a 4-1/2-digit display plus decimals and sign, or 25 lamps. A special technique allows driving 5 1/2 digits; see Figure 16. A configuration register allows the drive capability to be partitioned off to suit many additional applications. The on-chip decoder outputs 7-segment-format numerals 0 to 9, hexadecimal characters A to F, plus 15 letters and symbols.

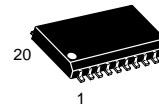
The MC14489 is compatible with the Motorola SPI and National MICRO-WIRE™ serial data ports. The chip's patented BitGrabber™ registers augment the serial interface by allowing random access without steering or address bits. A 24-bit transfer updates the display register. Changing the configuration register requires an 8-bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 6 V
- Operating Junction Temperature Range: -40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low-Resistance FET Switches Provide Direct Common Cathode Interface
- Low-Power Mode (Extinguishes the LEDs) and Brightness Controlled via Serial Port
- Special Circuitry Minimizes EMI when Display is Driven and Eliminates EMI in Low-Power Mode
- Power-On Reset (POR) Blanks the Display on Power-Up, Independent of Supply Ramp Up Time
- May Be Used with Double-Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)
- See Application Note AN431, *Temperature Measurement and Display Using the MC68HC05B4 and the MC14489* and Engineering Bulletin EB153, *Driving a Seven-Segment Display with the Neuron® Chip*

MC14489



P SUFFIX
PLASTIC DIP
CASE 738

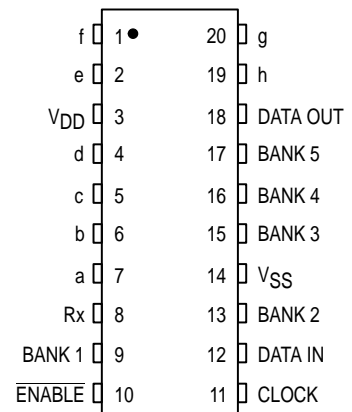


DW SUFFIX
SOG PACKAGE
CASE 751D

ORDERING INFORMATION

MC14489P Plastic DIP
MC14489DW SOG Package

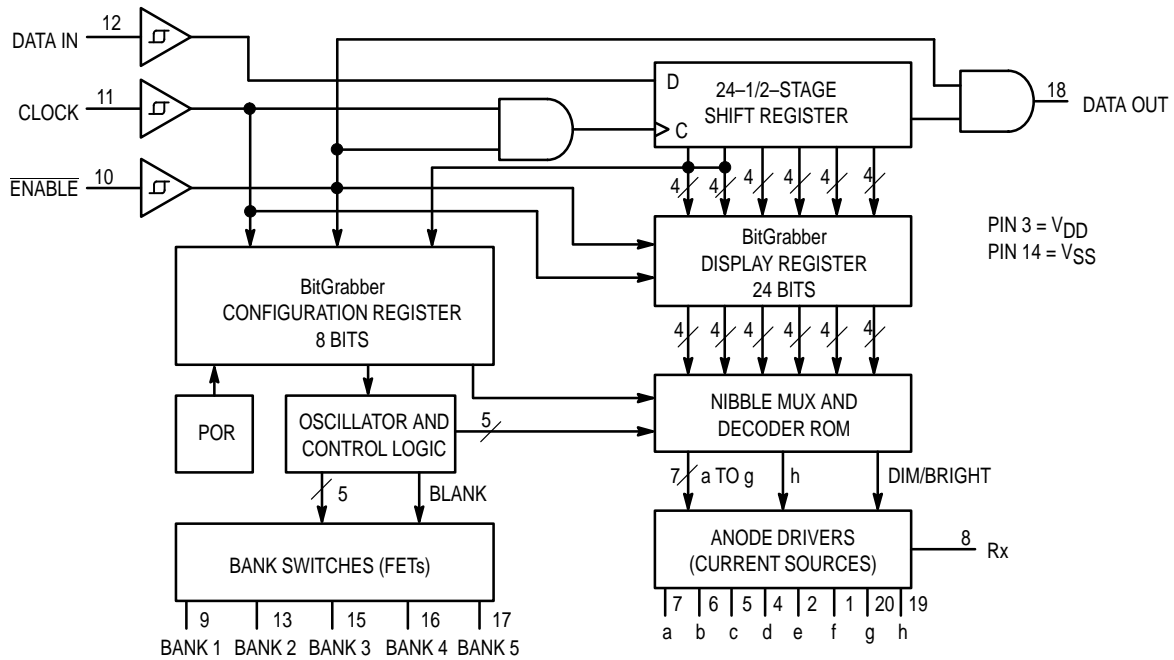
PIN ASSIGNMENT



See web site motorola.com/pll for PLL control software. Look under Overview/Support Products/PLL Demonstration Software. Choose PLLGEN.EXE. Although the MC14489 is not a PLL, the software available at the above location may be used with this part.

BitGrabber is a trademark of Motorola Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	- 0.5 to + 6.0	V
V_{in}	DC Input Voltage	- 0.5 to $V_{DD} + 0.5$	V
V_{out}	DC Output Voltage	- 0.5 to $V_{DD} + 0.5$	V
I_{in}	DC Input Current — per Pin (Includes Pin 8)	± 15	mA
I_{out}	DC Output Current — Pins 1, 2, 4 - 7, 19, 20 Sourcing	- 40	mA
	Sinking	10	
	Pins 9, 13, 15, 16, 17 Sinking	320	
	Pin 18	± 15	
I_{DD}, I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	± 350	mA
T_J	Chip Junction Temperature	- 40 to + 130	$^{\circ}C$
$R_{\theta JA}$	Device Thermal Resistance, Junction-to-Ambient (see Thermal Considerations section)	Plastic DIP	90
		SOG Package	100
T_{stg}	Storage Temperature	- 65 to + 150	$^{\circ}C$
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}C$

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS} , $T_J = -40^\circ$ to 130°C^* unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range of LED Drive Circuitry		—	4.5 to 6.0	V
V_{DD} (stby)	Minimum Standby Voltage	Bits Retained in Display and Configuration Registers, Data Port Fully Functional	—	3.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$)		3.0 6.0	0.9 1.8	V
V_{IH}	Minimum High-Level Input Voltage (Data In, Clock, $\overline{\text{Enable}}$)		3.0 6.0	2.1 4.2	V
V_{Hys}	Minimum Hysteresis Voltage (Data In, Clock, $\overline{\text{Enable}}$)		3.0 6.0	0.2 0.4	V
V_{OL}	Maximum Low-Level Output Voltage (Data Out)	$I_{out} = 20 \mu\text{A}$	3.0 6.0	0.1 0.1	V
		$I_{out} = 1.3 \text{ mA}$	4.5	0.4	
V_{OH}	Minimum High-Level Output Voltage (Data Out)	$I_{out} = -20 \mu\text{A}$	3.0 6.0	2.9 5.9	V
		$I_{out} = -800 \mu\text{A}$	4.5	4.1	
I_{in}	Maximum Input Leakage Current (Data In, Clock, $\overline{\text{Enable}}$)	$V_{in} = V_{DD}$ or V_{SS}	6.0	± 2.0	μA
		$V_{in} = V_{DD}$ or V_{SS} , $T_J = 25^\circ\text{C}$ only	6.0	± 0.1	
i_{OL}	Minimum Sinking Current (a, b, c, d, e, f, g, h)	$V_{out} = 1.0 \text{ V}$	4.5	0.2	mA
i_{OH}	Peak Sourcing Current — See Figure 7 for currents up to 35 mA (a, b, c, d, e, f, g, h)	$R_x = 2.0 \text{ k}\Omega$, $V_{out} = 3.0 \text{ V}$, Dimmer Bit = High	5.0	13 to 17.5	mA
		$R_x = 2.0 \text{ k}\Omega$, $V_{out} = 3.0 \text{ V}$, Dimmer Bit = Low	5.0	6 to 9	
I_{OZ}	Maximum Output Leakage Current (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	$V_{out} = V_{DD}$ (FET Leakage)	6.0	50	μA
		$V_{out} = V_{DD}$ (FET Leakage), $T_J = 25^\circ\text{C}$ only	6.0	1	
		$V_{out} = V_{SS}$ (Protection Diode Leakage)	6.0	1	
R_{on}	Maximum ON Resistance (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5)	$I_{out} = 0$ to 200 mA	5.0	10	Ω
I_{DD} , I_{SS}	Maximum Quiescent Supply Current	Device in Low-Power Mode, $V_{in} = V_{SS}$ or V_{DD} , Rx in Place, Outputs Open	6.0	100	μA
		Same as Above, $T_J = 25^\circ\text{C}$	6.0	20	
I_{ss}	Maximum RMS Operating Supply Current (The V_{SS} leg does not contain the Rx current component. See Pin Descriptions.)	Device NOT in Low-Power Mode, $V_{in} = V_{SS}$ or V_{DD} , Outputs Open	6.0	1.5	mA

* See Thermal Considerations section.

AC ELECTRICAL CHARACTERISTICS ($T_J = -40^\circ$ to 130°C^* , $C_L = 50$ pF, Input $t_r = t_f = 10$ ns)

Symbol	Parameter	V _{DD} V	Guaranteed Limit	Unit
f _{clk}	Serial Data Clock Frequency, Single Device or Cascaded Devices NOTE: Refer to Clock t _w below (Figure 1)	3.0 4.5 6.0	dc to 3.0 dc to 4.0 dc to 4.0	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Data Out (Figures 1 and 5)	3.0 4.5 6.0	140 80 80	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Data Out (Figures 1 and 5)	3.0 4.5 6.0	70 50 50	ns
f _R	Refresh Rate — Bank 1 through Bank 5 (Figures 2 and 6)	3.0 4.5 6.0	NA 700 to 1900 700 to 1900	Hz
C _{in}	Maximum Input Capacitance — Data In, Clock, $\overline{\text{Enable}}$	—	10	pF

* See Thermal Considerations section.

TIMING REQUIREMENTS ($T_J = -40^\circ$ to 130°C^* , Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V _{DD} V	Guaranteed Limit	Unit
t _{SU} , t _H	Minimum Setup and Hold Times, Data In versus Clock (Figure 3)	3.0 4.5 6.0	50 40 40	ns
t _{SU} , t _H , t _{REC}	Minimum Setup, Hold, ** and Recovery Times, $\overline{\text{Enable}}$ versus Clock (Figure 4)	3.0 4.5 6.0	150 100 100	ns
t _{w(L)}	Minimum Active–Low Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	4.5 3.4 3.4	μs
t _{w(H)}	Minimum Inactive–High Pulse Width, $\overline{\text{Enable}}$ (Figure 4)	3.0 4.5 6.0	300 150 150	ns
t _w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 6.0	167 125 125	ns
t _r , t _f	Maximum Input Rise and Fall Times — Data In, Clock, $\overline{\text{Enable}}$ (Figure 1)	3.0 4.5 6.0	1 1 1	ms

* See Thermal Considerations section.

** For a high-speed 8-Clock access, t_H for $\overline{\text{Enable}}$ is determined as follows:

$$V_{DD} = 3 \text{ to } 4.5 \text{ V, } f_{\text{clk}} > 1.78 \text{ MHz: } t_H = 4350 - (7500/f_{\text{clk}})$$

$$V_{DD} = 4.5 \text{ to } 6 \text{ V, } f_{\text{clk}} > 2.34 \text{ MHz: } t_H = 3300 - (7500/f_{\text{clk}})$$

where t_H is in ns and f_{clk} is in MHz.

NOTES:

1. This restriction does NOT apply for f_{clk} rates less than those listed above. For "slow" f_{clk} rates, use the t_H limits in the above table.
2. This restriction does NOT apply for an access involving more than 8 Clocks. For > 8 Clocks, use the t_H limits in the above table.

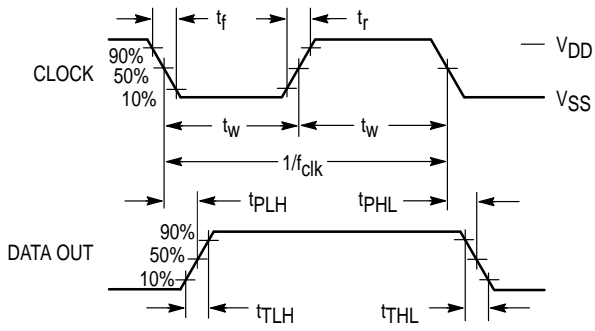


Figure 1.

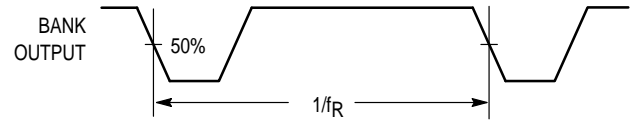


Figure 2.

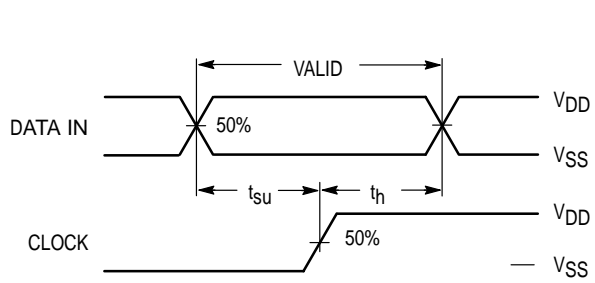


Figure 3.

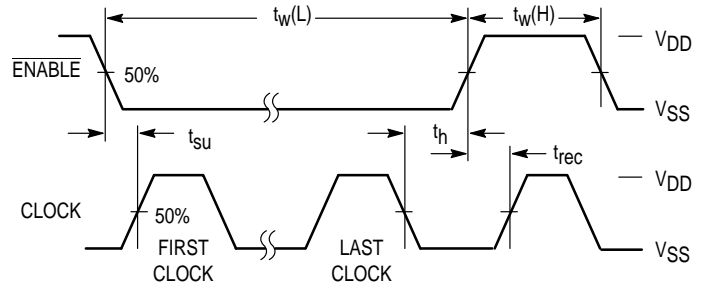


Figure 4.

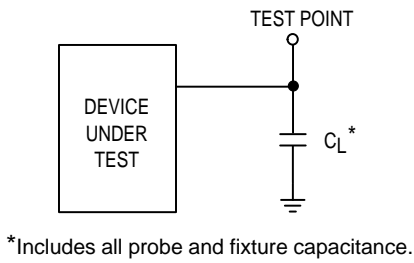


Figure 5.

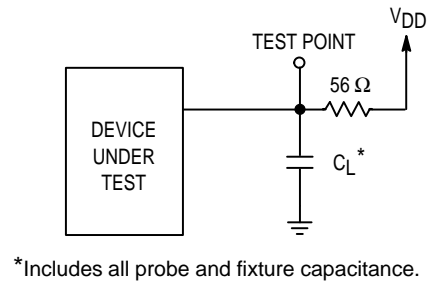


Figure 6.

PIN DESCRIPTIONS

DIGITAL INTERFACE

Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low-to-high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not change during shifting (until $\overline{\text{Enable}}$ makes a low-to-high transition) which allows slow serial data rates, if desired.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. Random access of either register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 3 to 6 V. Formats are shown in Figures 8 through 14 and summarized in Table 2. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 k Ω to 10 k Ω must be used. Parameters to be considered when sizing the resistor are the worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Clock (Pin 11)

Serial Data Clock Input. Low-to-high transitions on Clock shift bits available at Data In, while high-to-low transitions shift bits from Data Out. The chip's 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode. The Clock input does not need to be synchronous with the on-chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489 is not cascaded. See Figures 8 and 9.

As shown in Figure 10, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 10.

Cascading of 3, 4, 5, and 6 devices is shown in Figures 11, 12, 13, and 14, respectively. Also, reference Table 2.

Clock typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

NOTE

To guarantee proper operation of the power-on reset (POR) circuit, the Clock pin must NOT be floated or toggled during power-up. That is, the Clock pin must be **stable** until the V_{DD} pin reaches at least 3 V.

If control of the Clock pin during power-up is not practical, then the MC14489 must be reset via bit C0 in the C register. To accomplish this, C0 is reset low, then set high.

$\overline{\text{Enable}}$ (Pin 10)

Active-Low Enable Input. This pin allows the MC14489 to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{\text{Enable}}$ is in an inactive high state, Data Out is forced to a known (low) state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{Enable}}$ (which initially must be inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{\text{Enable}}$ is taken high. The low-to-high transition on $\overline{\text{Enable}}$ transfers data to either the configuration or display register, depending on the data stream length.

Every rising edge on $\overline{\text{Enable}}$ initiates a blanking interval while data is loaded. Thus, continually loading the device with the same data may cause the LEDs on some banks to appear dimmer than others.

NOTE

Transitions on $\overline{\text{Enable}}$ must not be attempted while Clock is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{Enable}}$ is high and Clock is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD} , thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high-to-low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489's, Data Out feeds Data In of the next device per Figures 10, 11, 12, 13, and 14.

Data Out could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power-up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in-line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

DISPLAY INTERFACE

Rx (Pin 8)

External Current-Setting Resistor. A resistor tied between this pin and ground (V_{SS}) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having $\pm 1\%$ tolerance should be used. See Figure 7.

CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **Thermal Considerations**.

a through h (Pins 1, 2, 4 – 7, 19, 20)

Anode–Driver Current Sources. These outputs are closely–matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs. Each output is capable of sourcing up to 35 mA.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 17.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. Refer to Figure 9. If unused, h must be left open.

Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)

Diode–Bank FET Switches. These outputs are low–resistance switches to ground (V_{SS}) capable of handling currents of up to 320 mA each. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on–chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

POWER SUPPLY

V_{SS} (Pin 14)

Most–negative supply potential. This pin is usually ground.

Resistor Rx is externally tied to ground (V_{SS}). Therefore, the chip's V_{SS} pin does not contain the Rx current component.

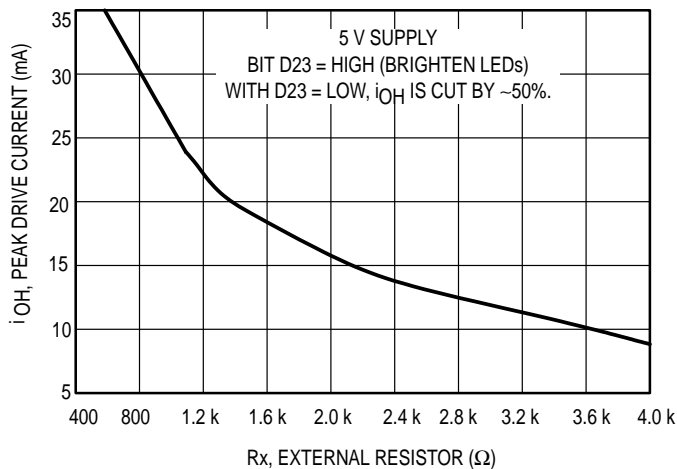
V_{DD} (Pin 13)

Most–positive supply potential.

To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to V_{SS} . For example, within this voltage range, the chip could be placed in and out of the low–power mode.

To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to V_{SS} .

The V_{DD} pin contains the Rx current component plus the chip's current drain. In the low–power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the V_{DD} current, I_{DD} .



NOTE: Drive current tolerance is approximately $\pm 15\%$.

Figure 7. a through h Nominal Current per Output versus Rx

Table 1. Triple-Mode Segment Decoder Function Table

Bank Nibble Value		7-Segment Display Characters		Lamp Conditions			
				No Decode ^① (Invoked via Bits C1 to C7)			
Hexadecimal	Binary MSB LSB	Hex Decode (Invoked via Bits C1 to C5)	Special Decode (Invoked via Bits C1 to C7)	d	c	b	a
\$0	L L L L	0					
\$1	L L L H	1	c				on
\$2	L L H L	2	H			on	
\$3	L L H H	3	h			on	on
\$4	L H L L	4	J		on		
\$5	L H L H	5 ^②	L		on		on
\$6	L H H L	6	n		on	on	
\$7	L H H H	7	o		on	on	on
\$8	H L L L	8 ^③	P	on			
\$9	H L L H	9 ^④	r	on			on
\$A	H L H L	A	U	on		on	
\$B	H L H H	b	u	on		on	on
\$C	H H L L	C	y	on	on		
\$D	H H L H	d	-	on	on		on
\$E	H H H L	E	-	on	on	on	
\$F	H H H H	F	o	on	on	on	on

NOTES:

- In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:
 - Individually controlling lamps.
 - Controlling a half digit with sign.
 - Controlling annunciators - examples: AM, PM, UHF, kV, mm Hg.
- Can be used as capital S.
- Can be used as capital B.
- Can be used as small g.

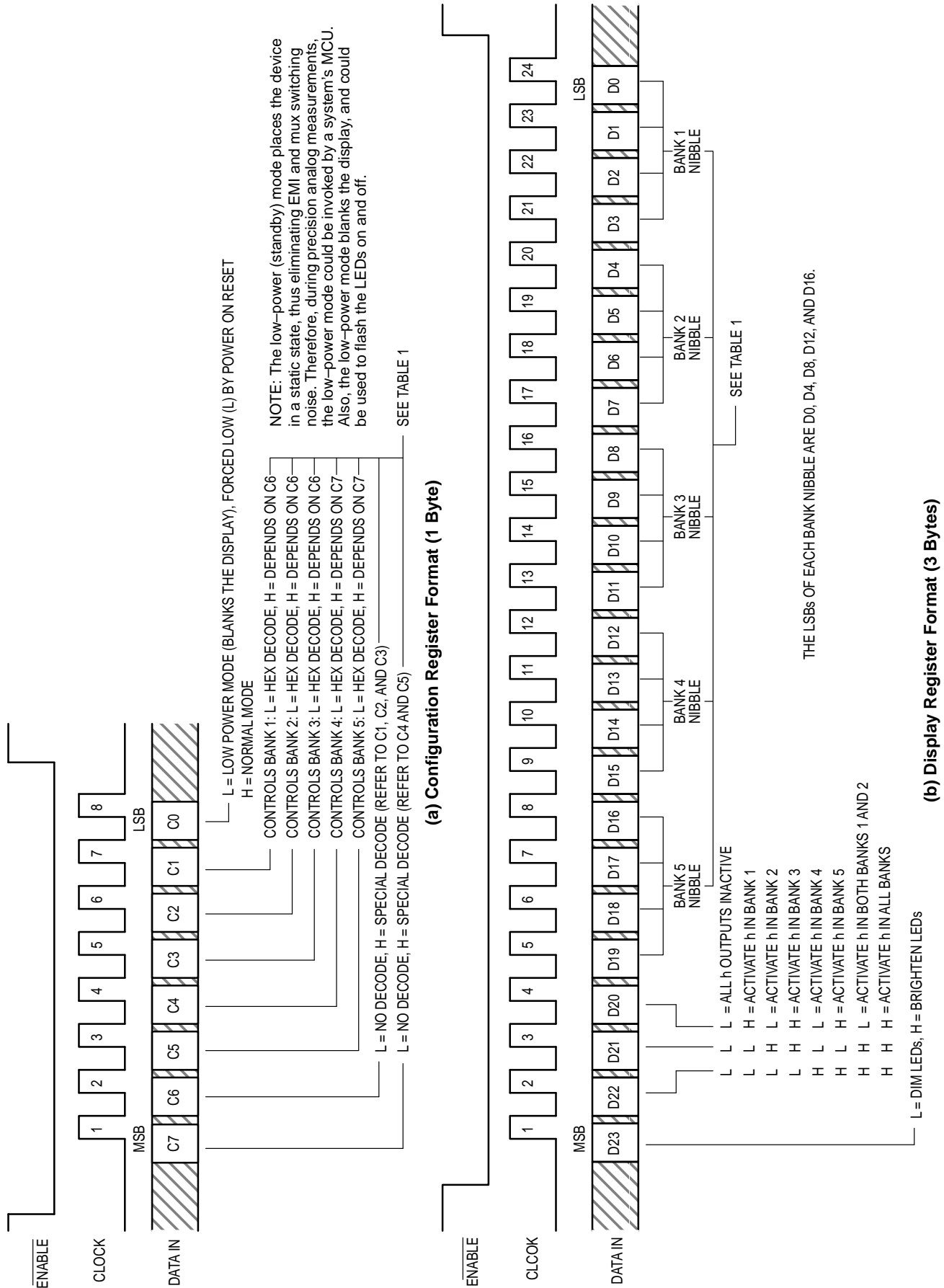


Figure 8. Timing Diagrams for Non-Cascaded Devices

APPLICATIONS INFORMATION

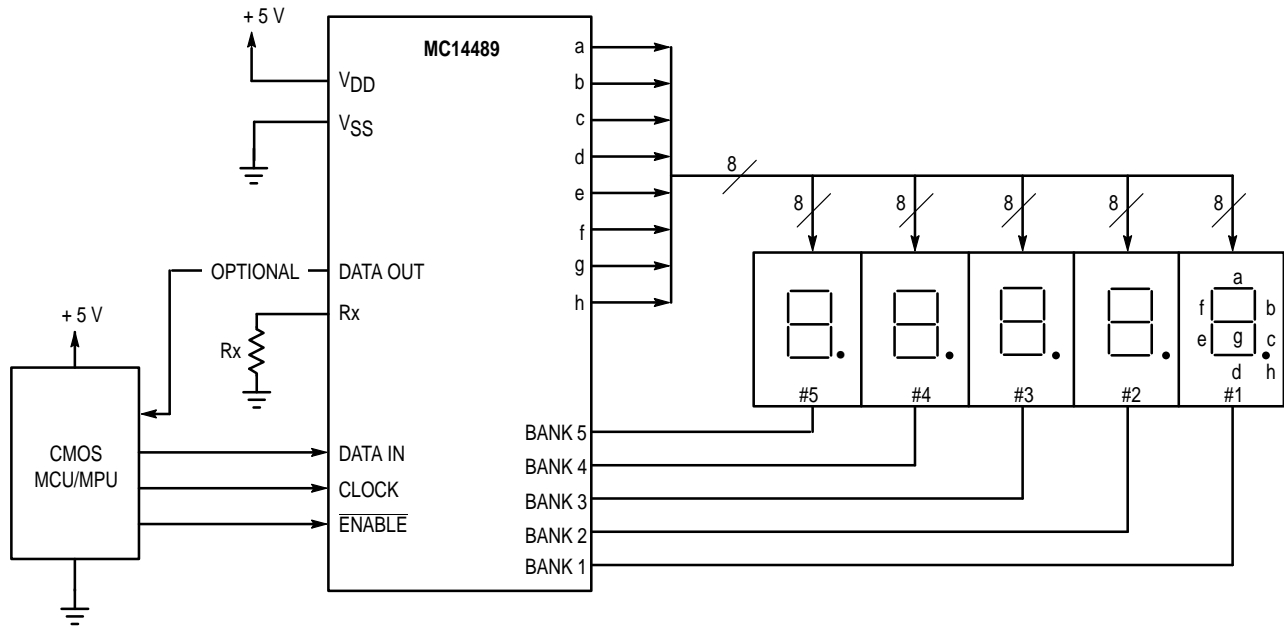


Figure 9. Non-Cascaded Application Example: 5 Character Common Cathode LED Display with Two Intensities as Controlled via Serial Port

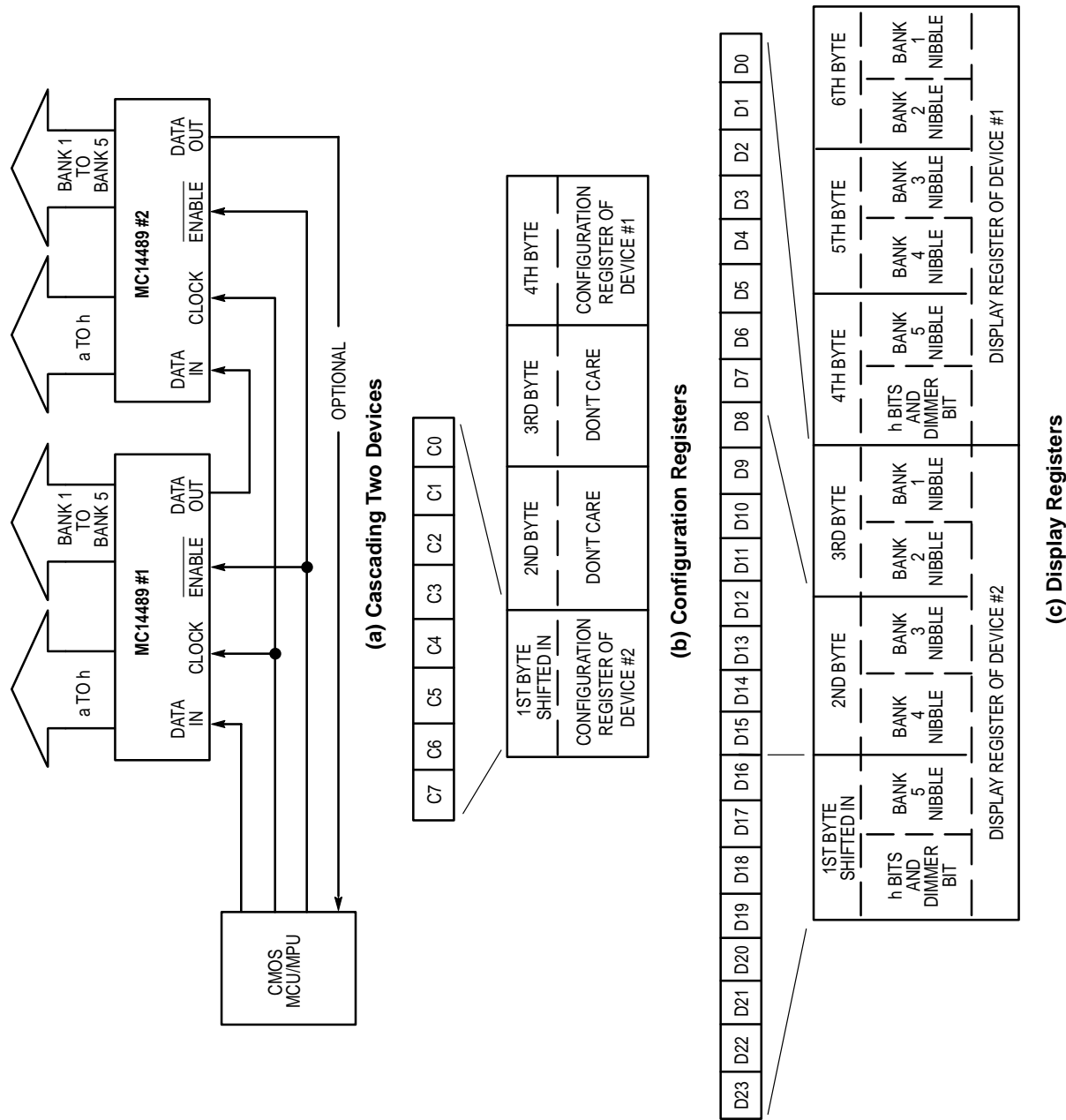
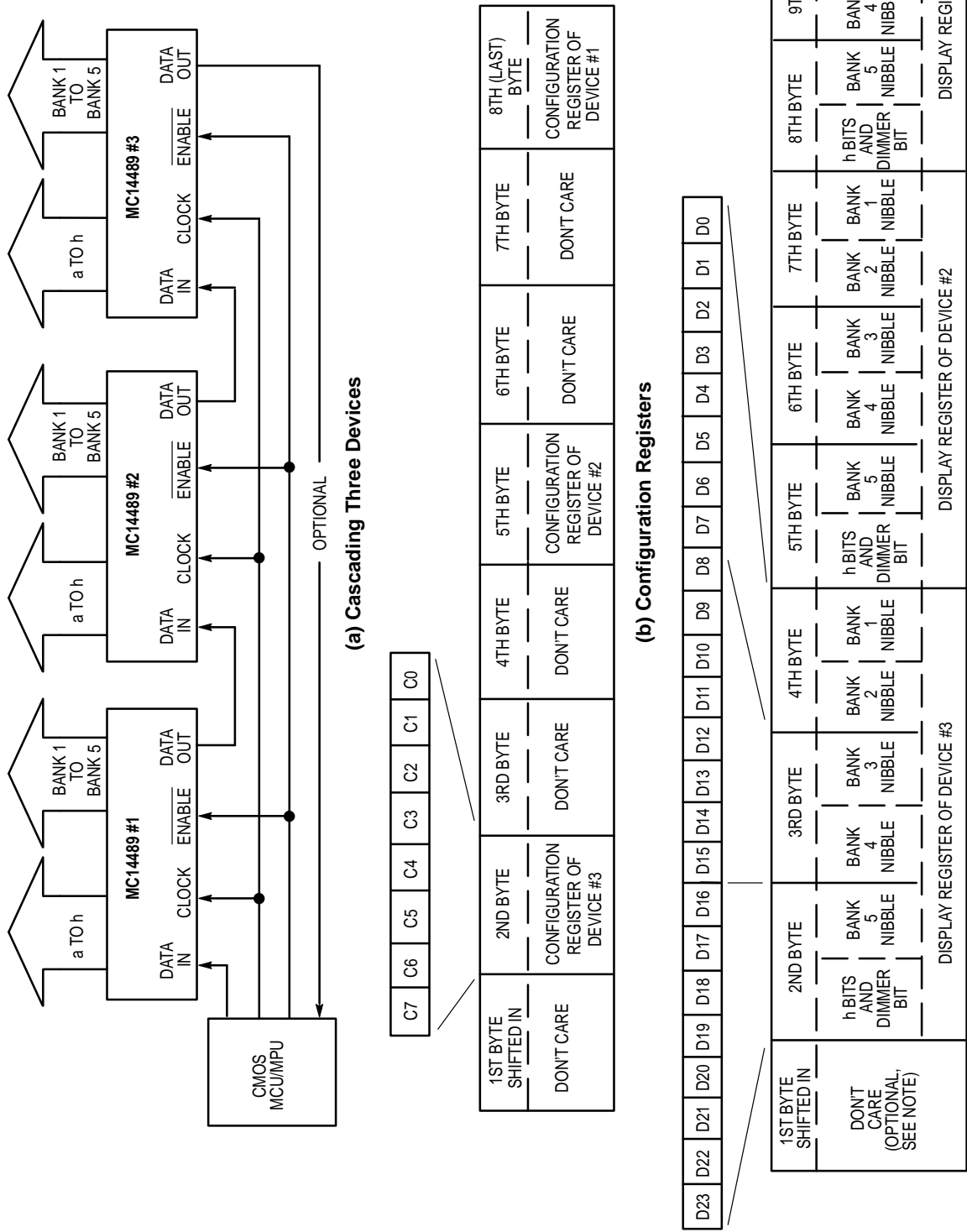


Figure 10. Bit Stream Formats for Two Devices Cascaded

NOTE: ENABLE (which initially must be inactive high) is kept active-low during the entire 4-byte configuration transfer or 6-byte display transfer. When ENABLE is brought back high, either a 4- or 6-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.



NOTE: When the leading "don't care" bytes are included, ENABLE (which initially must be inactive high) is kept active-low during the entire 8-byte configuration transfer or 10-byte display transfer. When ENABLE is brought back high, either an 8- or 10-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the one "don't care" byte can be eliminated as follows: (1) take ENABLE active low, (2) transfer 6 bytes, (3) pulse ENABLE inactive high, see $t_{w(H)}$ spec, (4) transfer last 3 bytes, and (5) take ENABLE inactive high.

Figure 11. Bit Stream Formats for Three Devices Cascaded

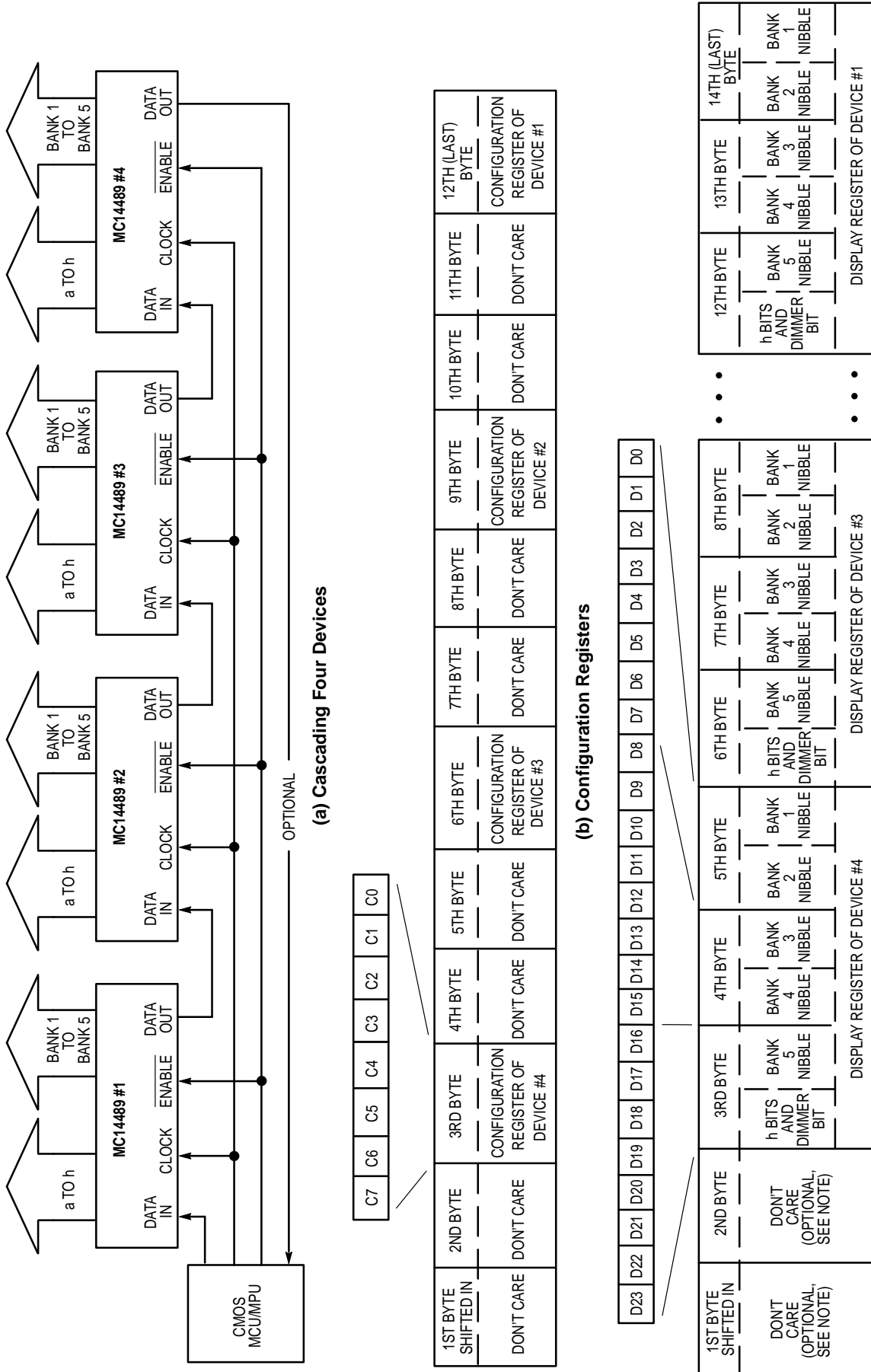


Figure 12. Bit Stream Formats for Four Devices Cascaded

NOTE: When the leading "don't care" bytes are included, ENABLE (which initially must be inactive high) is kept active-low during the entire 12-byte configuration transfer or 14-byte display transfer. When ENABLE is brought back high, either a 12- or 14-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the two "don't care" bytes can be eliminated as follows: (1) take ENABLE active low, (2) transfer 6 bytes, (3) pulse ENABLE inactive high, see $t_{w(H)}$ spec, (4) transfer last 6 bytes, and (5) take ENABLE inactive high.

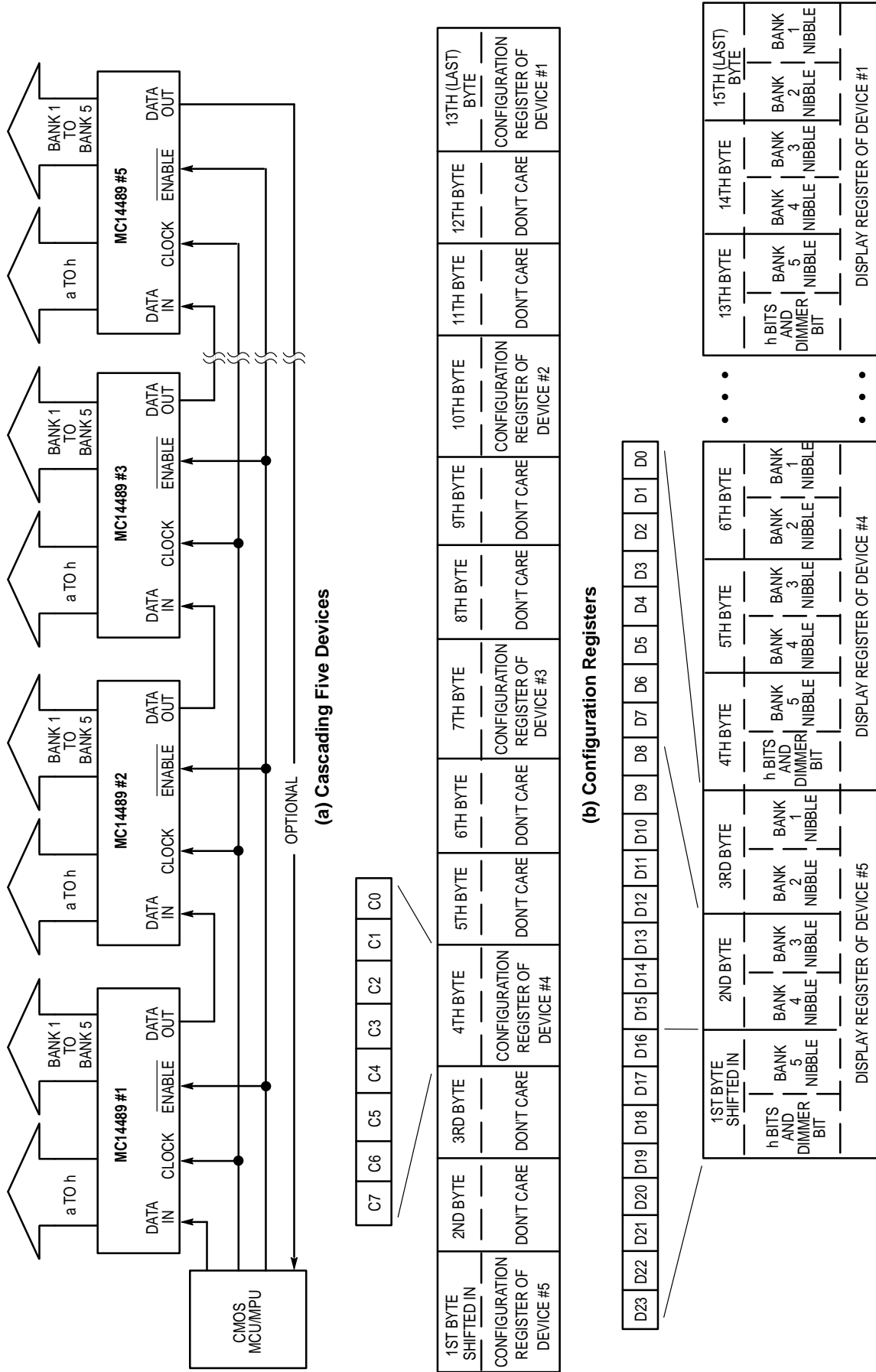


Figure 13. Bit Stream Formats for Five Devices Cascaded

NOTE: ENABLE (which initially must be inactive high) is kept active-low during the entire 13-byte configuration transfer or 15-byte display transfer. When ENABLE is brought back high, either a 13- or 15-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

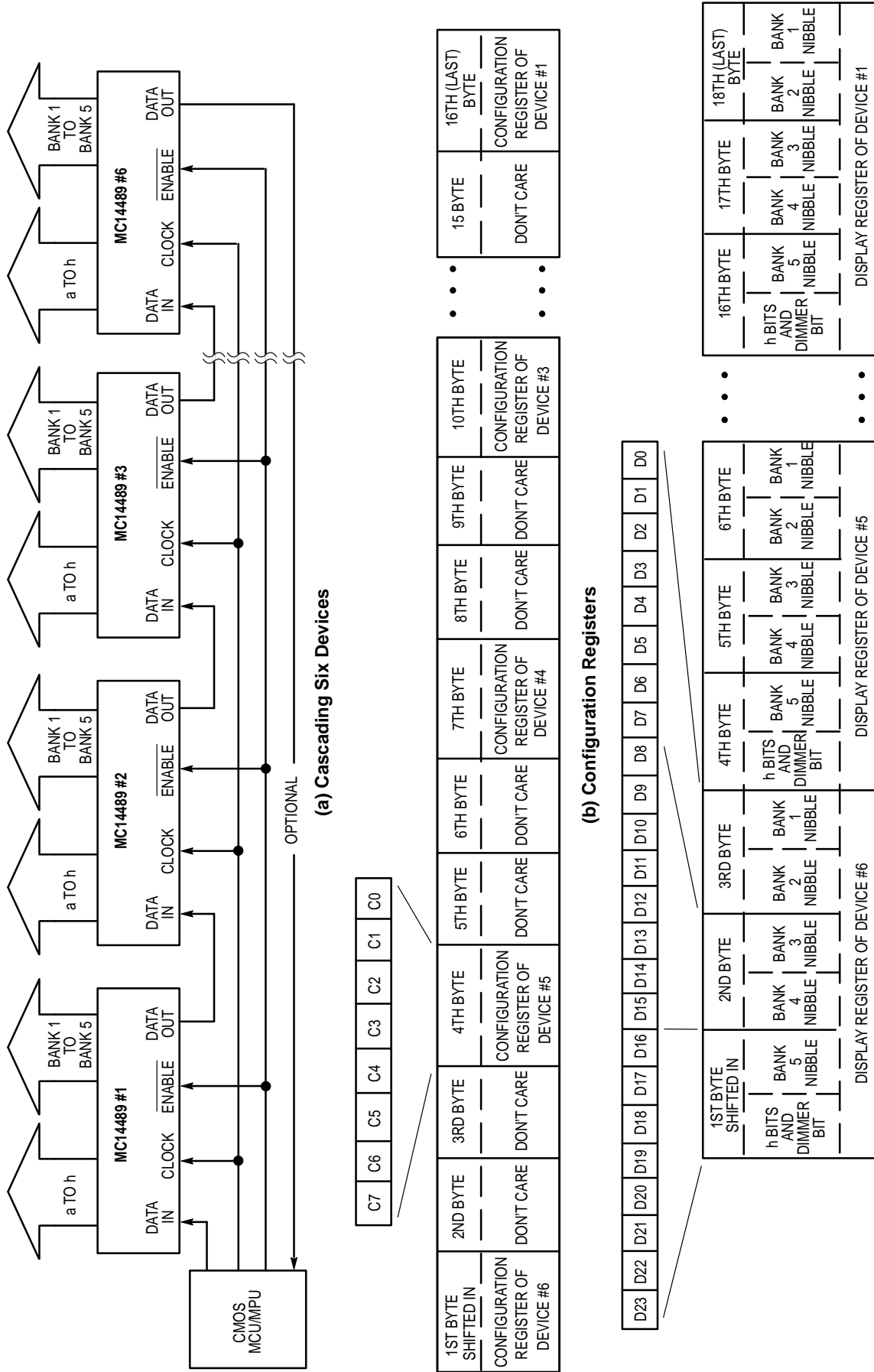


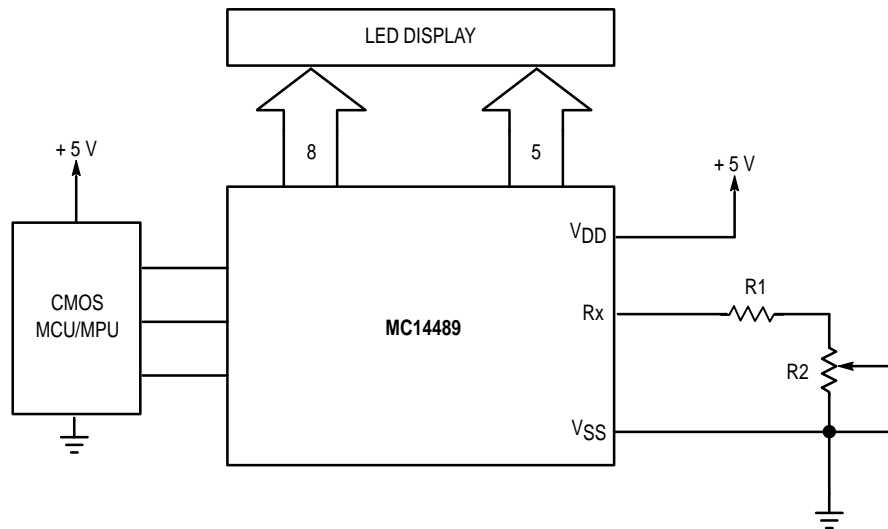
Figure 14. Bit Stream Formats for Six Devices Cascaded

NOTE: ENABLE (which initially must be inactive high) is kept active-low during the entire 16-byte configuration transfer or 18-byte display transfer. When ENABLE is brought back high, either a 16- or 18-byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

Table 2. Register Access for Two or More Cascaded Devices

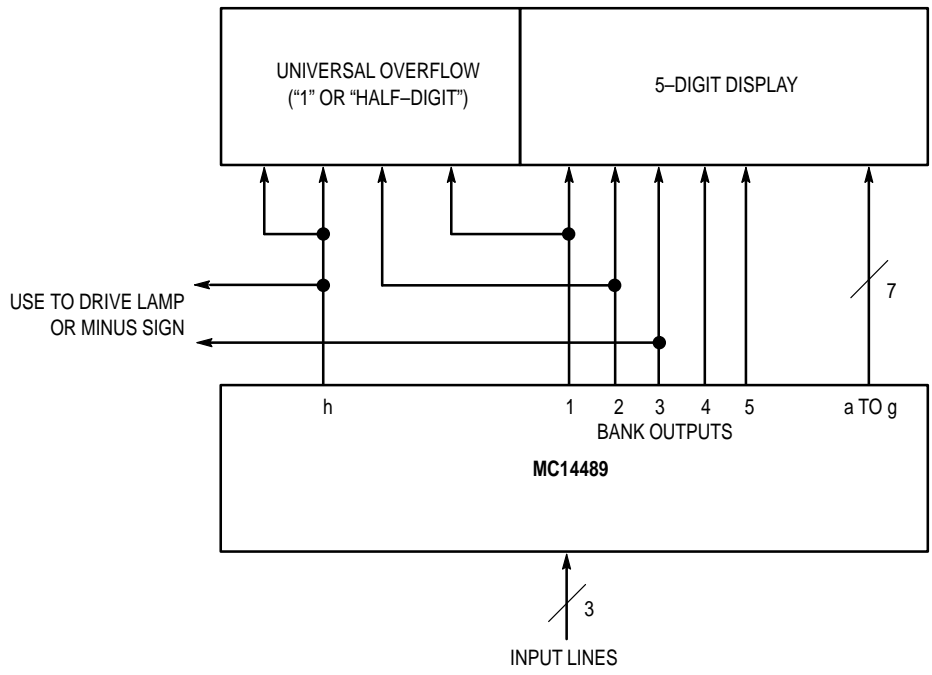
Criteria*	Configuration Register Access		Display Register Access	
	Total Number of Bytes	Number of Leading "Don't Care" Bytes	Total Number of Bytes	Number of Leading "Don't Care" Bytes
If $3N$ is a Multiple of 4	$3N$	2	$3N + 2$	2
If $3N - 1$ is a Multiple of 4	$3N - 1$	1	$3N + 1$	1
If $3N - 2$ is a Multiple of 4	$3N - 2$	0	$3N$	0
If $3N - 3$ is a Multiple of 4	$3N - 2$	0	$3N$	0

* N = number of devices that are cascaded. For example, to drive 10 digits, 2 devices are cascaded; therefore, N = 2. To drive 35 digits, seven devices are cascaded; therefore N = 7.



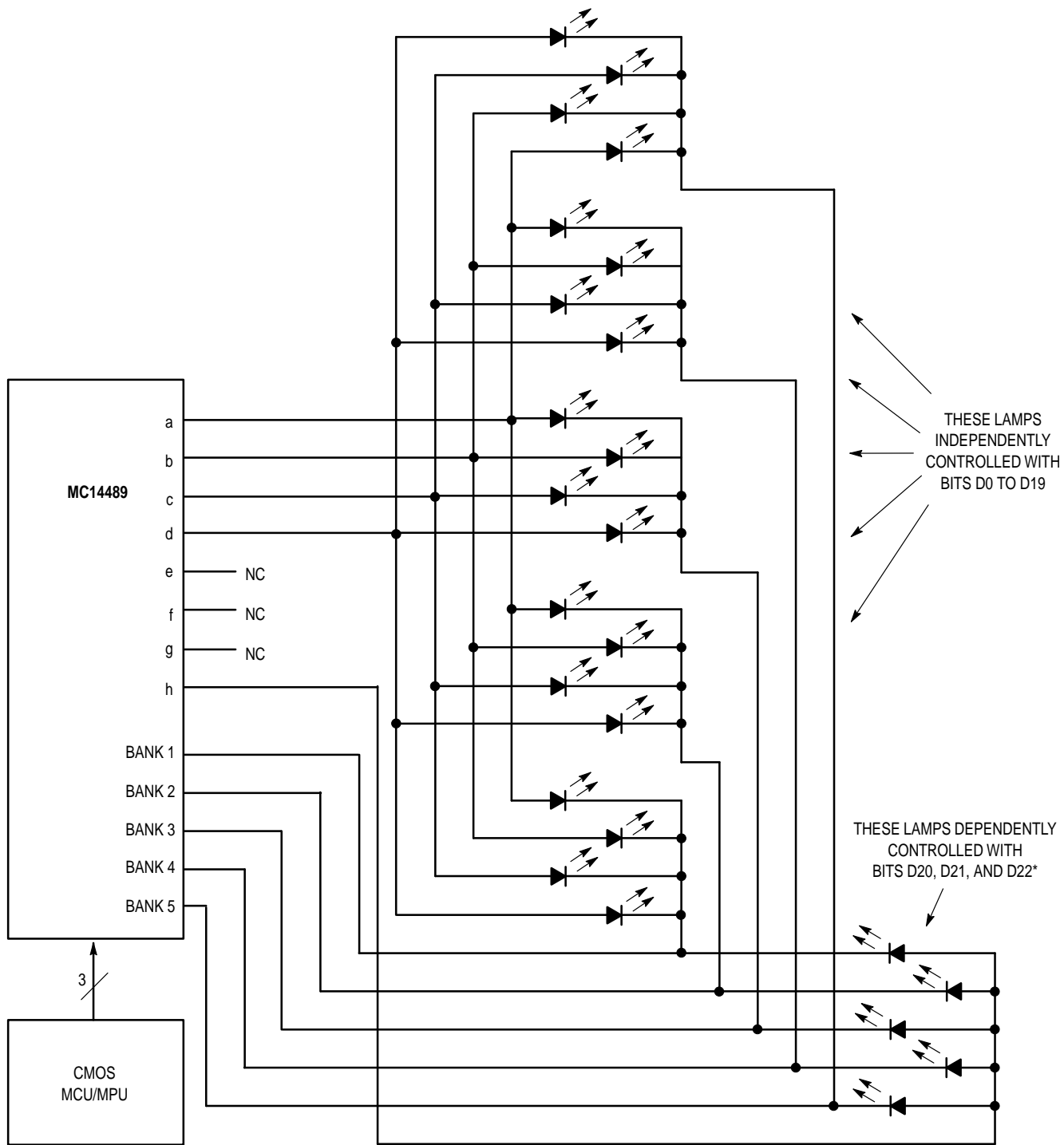
NOTE: R1 limits the maximum current to avoid damaging the display and/or the MC14489 due to overheating. See the Thermal Considerations section. An 1/8 watt resistor may be used for R1. R2 is a 1 kΩ or 5 kΩ potentiometer (≥ 1/8 watt). R2 may be a light-sensitive resistor.

Figure 15. Common-Cathode LED Display with Dial-Adjusted Brightness



NOTE: A Universal Overflow pins out all anodes and cathodes.

Figure 16. Driving 5 1/2 Digits



* If required, this group of lamps can be independently controlled. To accomplish independent control, only connect lamps to BANK 1 and BANK 2 for output h (two lamps). Then, use bits D20, D21, and D22 for control of these two lamps.

Figure 17. 25-Lamp Application

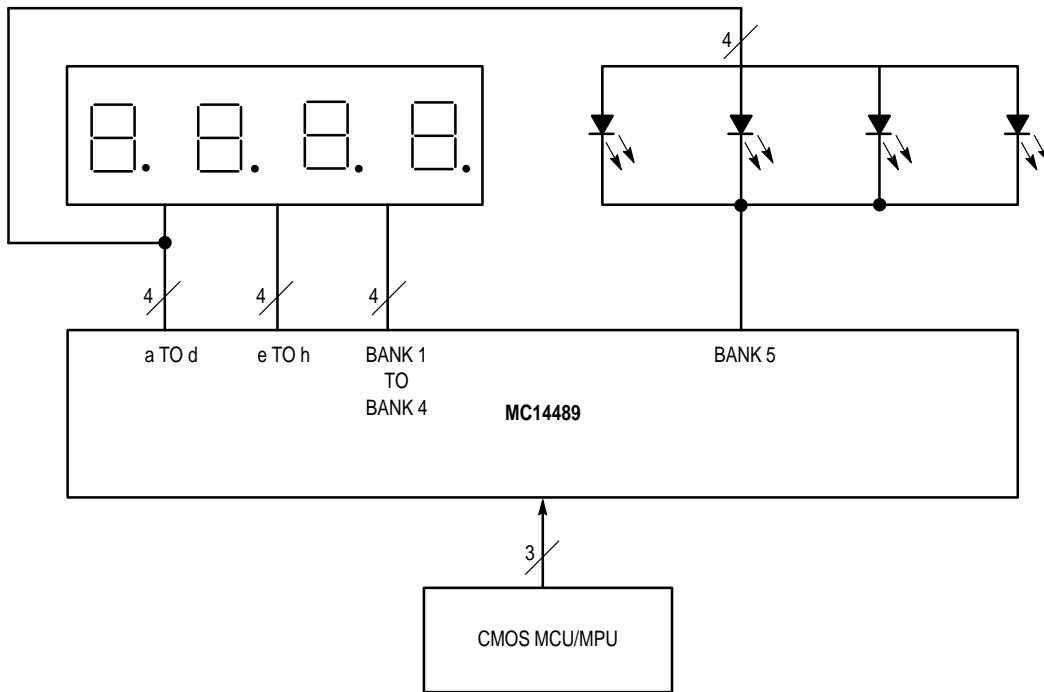


Figure 18. 4-Digit Display Plus Decimals with Four Annunciators or 4-1/2-Digit Display Plus Sign

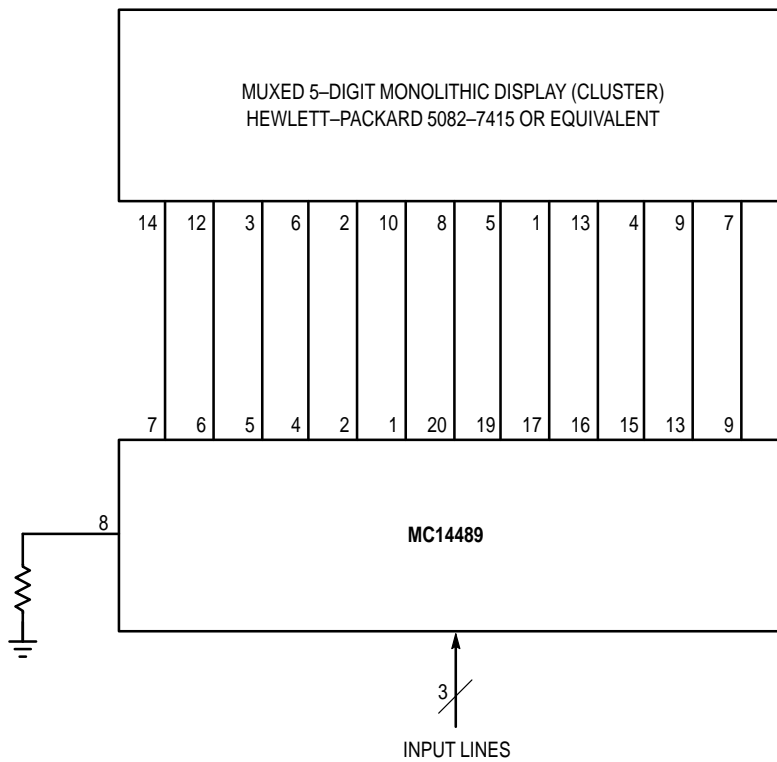


Figure 19. Compact Display System with Three Components

THERMAL CONSIDERATIONS

The MC14489 is designed to operate with a *chip-_junction* temperature (T_J) ranging from -40 to 130°C , as indicated in the electrical characteristics tables. The *ambient* operating temperature range (T_A) is dependent on $R_{\theta JA}$, the internal chip current, how many anode drivers are used, the number of bank drivers used, the drive current, and how the package is cooled. The maximum ratings table gives the thermal resistance, junction-to-ambient, of the MC14489 mounted on a pc board using natural convection to be 90°C per watt for the plastic DIP. The SOG thermal resistance is 100°C per watt.

The following general equation (1) is used to determine the power dissipated by the MC14489.

$$P_T = P_D + P_I \quad (1)$$

where

- P_T = Total power dissipation of the MC14489
- P_D = Power dissipated in the driver circuitry (mW)
- P_I = Power dissipated by the internal chip circuitry (mW)

The equations for the two terms of the general equation are:

$$P_D = (i_{OH})(N)(V_{DD} - V_{LED})(B/5) \quad (2)$$

$$P_I = (1.5 \text{ mA})(V_{DD}) + I_{R_x}(V_{DD} - I_{R_x}R_x) \quad (3)$$

where

- i_{OH} = Peak anode driver current (mA)
- I_{R_x} = $i_{OH}/10$, with i_{OH} = the peak anode driver current (mA) when the dimmer bit is high
- N = Number of anode drivers used
- B = Number of bank drivers used
- R_x = External resistor value ($k\Omega$)
- V_{DD} = Maximum supply voltage, referenced to V_{SS} (volts)
- V_{LED} = Minimum anticipated voltage drop across the LED
- 1.5 mA = Operating supply current of the MC14489

The following two examples show how to calculate the maximum allowable ambient temperature.

Worst-Case Analysis Example 1:

5-digit display with decimals (5 banks and 8 anode drivers)
DIP without heat sink on PC board

- $i_{OH} = 20 \text{ mA max}$
- $V_{LED} = 1.8 \text{ V min}$
- $V_{DD} = 5.25 \text{ max}$

$$P_D = (20)(8)(5.25 - 1.8)(5/5) = 552 \text{ mW} \quad \text{Ref. (2)}$$

$$P_I = (1.5)(5.25) + 2[5.25 - 2(2)] = 10 \text{ mW} \quad \text{Ref. (3)}$$

$$\text{Therefore, } P_T = 552 + 10 = 562 \text{ mW} \quad \text{Ref. (1)}$$

$$\text{and } \Delta T_{\text{chip}} = R_{\theta JA}P_T = (90^\circ\text{C/W})(0.562) = 51^\circ\text{C}$$

Finally, the maximum allowable

$$T_A = T_{J\text{max}} - \Delta T_{\text{chip}} = 130 - 51 = 79^\circ\text{C}$$

That is, if $T_A = 79^\circ\text{C}$, the maximum junction temperature is 130°C . The chip's average temperature for this example is lower than 130°C because all segments are usually not illuminated simultaneously for an indefinite period.

Worst-Case Analysis Example 2:

16 lamps (4 banks and 4 anode drivers)
SOG without heat sink on PC board

- $i_{OH} = 30 \text{ mA max}$
- $V_{LED} = 1.8 \text{ V min}$
- $V_{DD} = 5.5 \text{ max}$

$$P_D = (30)(4)(5.5 - 1.8)(4/5) = 355 \text{ mW} \quad \text{Ref. (2)}$$

$$P_I = (1.5)(5.5) + 3[5.5 - 3(1.0)] = 16 \text{ mW} \quad \text{Ref. (3)}$$

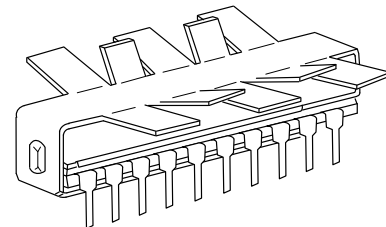
$$\text{Therefore, } P_T = 355 + 16 = 371 \text{ mW} \quad \text{Ref. (1)}$$

$$\text{and } \Delta T_{\text{chip}} = R_{\theta JA}P_T = (100^\circ\text{C/W})(0.371) = 37^\circ\text{C}$$

Finally, the maximum allowable

$$T_A = T_{J\text{max}} - \Delta T_{\text{chip}} = 130 - 37 = 93^\circ\text{C}$$

To extend the allowable ambient temperature range or to reduce T_J , which extends chip life, a heat sink such as shown in Figure 20 can be used in high-current applications. Alternatively, heat-spreader techniques can be used on the PC board, such as running a wide trace under the MC14489 and using thermal paste. Wide, radial traces from the MC14489 leads also act as heat spreaders.



AAVID #5804 or equivalent
(Tel. 603/524-4443, FAX 603/528-1478)
Motorola cannot recommend one supplier over another and in no way suggests that this is the only heat sink supplier.

Figure 20. Heat Sink

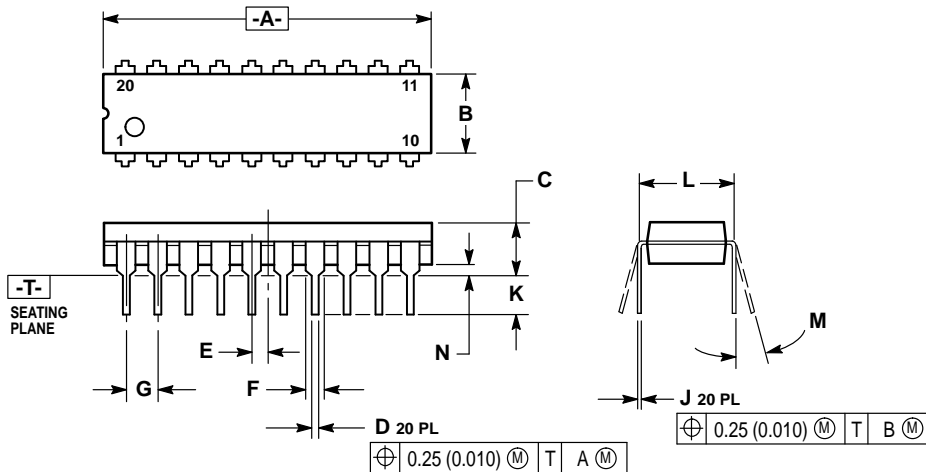
Table 3. LED Lamp and Common-Cathode Display Manufacturers

Supplier
QT Optoelectronics
Hewlett-Packard (HP), Components Group
Industrial Electronic Engineers (IEE), Component Products Div.
Purdy Electronics Corp., AND Product Line

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

PACKAGE DIMENSIONS

P SUFFIX PLASTIC DIP CASE 738-03

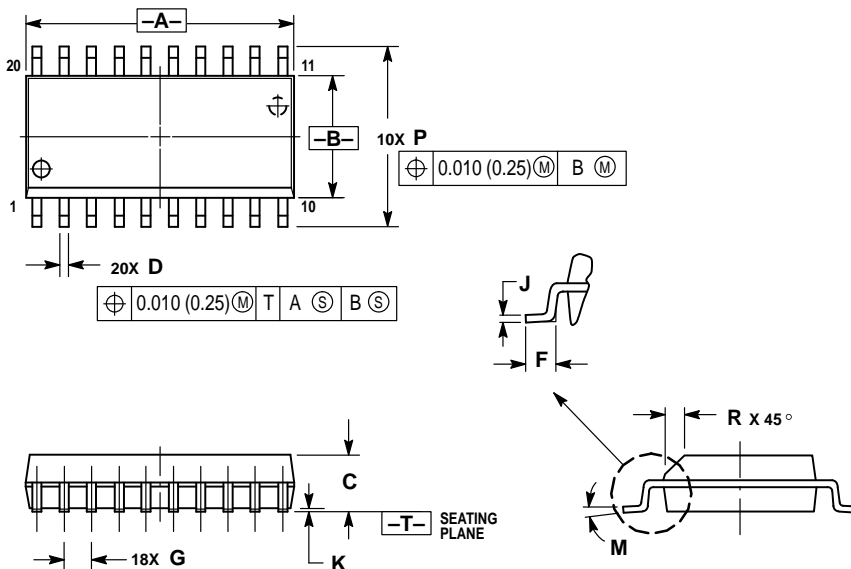


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01


DW SUFFIX SOG PACKAGE CASE 751D-04



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; SPD, Strategic Planning Office, 141,
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 81-3-5487-8488

Customer Focus Center: 1-800-521-6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848
– http://sps.motorola.com/mfax/

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

HOME PAGE: <http://motorola.com/sps/>

