FGEN1

DIGITAL FUNCTION GENERATOR CIRCUIT BOARD

USER'S MANUAL

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1.0 Introduction

The Digital Function Generator (FGEN) is designed to provide arbitrary audio frequency signals with high resolution. The FGEN can be set to precise values and is as stable as its master crystal oscillator. The available frequency range is 0.1 Hz to 20 kHz with 0.1 Hz resolution. The Waveform and Frequency can be controlled via the front panel (two switches and two push-buttons) or via RS-232. The front panel switches are not active while in Host Mode. Gain and Offset potentiometers on the front panel are always active. The FGEN can be used for a variety of applications requiring audio frequency stimulus.

1.1 Specifications

OUTPUT

- Output (PCB-J6)
  - DC coupled, BNC connector, 50 ohms

WAVEFORMS

- Fourteen waveforms (00-13) can be permanently stored in onboard EEPROM.
- Waveforms can be added or deleted from permanent storage using Host Mode.
- Frequency is adjustable from 0.1 Hz to 20 kHz with 0.1 Hz resolution.

MODES

- Manual Mode
  - Waveform selection and Frequency are controlled from front panel switches.
- Host Mode
  - Initiated by connection of RS-232 cable to PCB-J4.
  - Required for management of waveform files in permanent storage.
  - Options are selected via a terminal program running on the Host computer.

CONTROLS

- Filter bypass toggle switch - bypasses automatic filter bank selection.
- Line toggle switch - moves LCD cursor to upper or lower line.
- Advance pushbutton - on the Frequency line, it moves the LCD cursor right to the next numeric character; it has no effect on the Waveform line. The cursor wraps around to the first numeric character after reaching the right-most numeric character.
- Increment pushbutton - increments the numeric character at the LCD cursor. Numeric values wrap around from 9 to 0.
- Gain potentiometer (PCB-J1) - can vary the gain from 0.85 to 2.0.
- Offset potentiometer (PCB-J7) - can vary the offset ±0.83 volts.

POWER

- PCB connector J2, 5.5 mm diameter with 2.1 mm diameter center pin, center positive.
- External power, 9 volts DC at 100 mA.

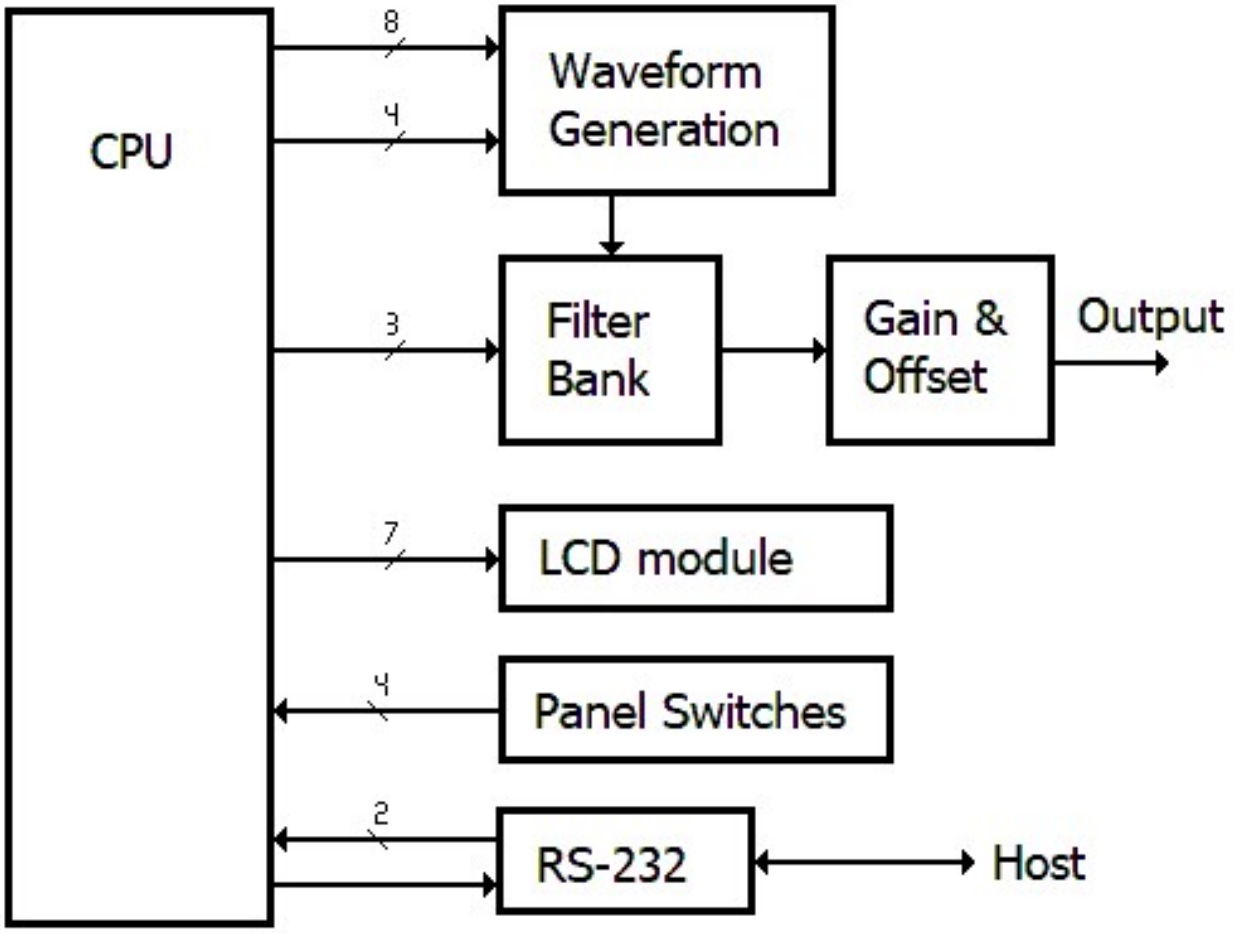


Figure 2.0. Block diagram of the FGEN

2.0 Circuit Description

This section describes the circuitry on the FGEN1 circuit board.

2.1 Power Supply

Schematic sheet 5 shows the power supply circuitry. The external 9 VDC input goes to two 78M05 linear voltage regulators, U10 and U11. Header SW1 allows the use of a power switch; otherwise a jumper should be placed at SW1 and connection/disconnection of the external 9 VDC supply will turn the FGEN1 on/off respectively. The voltage regulators are positioned on the board so that they can share a common heatsink. U10 supplies power to the digital circuitry while U11 supplies power to the analog circuitry. Analog and digital grounds join at the voltage regulators.

2.2 Microcontroller and Memory

The PIC16F18875 microcontroller, or PIC for short, is designated as U1 on sheet 1 of the schematics. This 40-pin PIC has 8192 words of flash program memory, 1024 bytes of data memory (RAM), 256 bytes of EEPROM memory, a 16-bit timer with prescaler (TMR1), an internal clock

oscillator, a universal asynchronous receiver transmitter (UART), a master synchronous serial port, a numerically controlled oscillator and 36 multi-functional input/output (I/O) lines. Lucid Technologies' FGEN firmware is programmed in the PIC's flash memory.

The 25LC320 chip (U2) is also shown on sheet 1 of the schematics. This is a SPI interface EEPROM with 32K bits of storage organized as 4K bytes. The EEPROM can store 14 waveform files numbered 00-13. At power up, the waveform stored in position 00 is output.

There are three places in the FGEN where waveform files may reside:

1. The **EEPROM** provides nonvolatile storage for waveform files.
2. The **Output RAM** contains the current waveform file. This will be discussed further in the Waveform Generation section.
3. The **PIC RAM** buffers waveform files while they are being moved from one place to another - such as from the EEPROM to the Output RAM.

2.2.1 Numerically Controlled Oscillator and Clock

The PIC's Numerically Controlled Oscillator (NCO) is the basis for the FGEN's frequency control. The NCO has a 20-bit phase-increment value which is added to the 20-bit phase-accumulator every NCO clock cycle. Overflows of the phase accumulator generate a pulse on the NCO output pin. The PIC's NCO output feeds an 8-bit counter in the waveform generation circuitry; this makes the effective phase accumulator (the count for one cycle of the output waveform) 28 bits. The NCO resolution, which is the frequency change when the phase-increment equals 1 is: Resolution = (NCO_clock) / (2^28). For a resolution of 0.1 Hz the equation becomes: 0.1 * (2^28) = NCO_clock = 26,843,545 Hz. The custom clock oscillator, Y1 on schematic sheet 1, that feeds the PIC operates at 26.8435 MHz which means the FGEN's frequency resolution is approximately 0.1 Hz.

2.3 Waveform Generation

The waveform generation circuitry is shown on sheet 2 of the schematics. The digital portion of this circuitry is composed of a 74HC4040, ripple counter (U3); a 74HC573, octal transparent latch with 3-state outputs (U4); and a 6116, 2Kx8 static RAM (U5). Only eight bits of the 74HC4040's twelve outputs are used; this 8-bit count goes through the 256 equally spaced phase values in one cycle of the output waveform. This phase count continues to rollover, repeating the periodic output waveform, as long as the NCO output from the PIC is active. Because the 74HC4040 is a *ripple* counter, its outputs don't all change simultaneously. The NCO output pulse increments the 74HC4040 and causes the 74HC573 to latch the last phase count while the 74HC4040 output ripples. At the end of the NCO output pulse the new, stable, phase count is presented to the 6116 static RAM address lines. Only eight of the 6116's eleven address lines are used because only 256 memory locations are needed. The 6116 RAM is called the **Output RAM**. Even though the 6116 has more memory than needed, it was used because a smaller parallel I/O static RAM was not available. As the phase count increments, the 256 bytes in the 6116 RAM, which are the voltage values of the waveform, are sequentially output on the RAM's eight data pins. The eight 6116 RAM outputs connect to the R-2R resistor network inputs.

During normal operation the PIC holds the Output RAM in Read-mode with output enabled. When it comes time to put a new waveform into the Output RAM, the PIC disconnects the NCO from the NCO output pin, clears the 74HC4040 ripple counter and disables the 6116 output. The

PIC then changes Port-B to output and sequentially presents the new 256 waveform values on Port-B while incrementing the 74HC4040 ripple counter and toggling the Output RAM's Write pin. After the new waveform is written to the Output RAM, Port-B is returned to a high-impedance input, the Output RAM is put back in Read-mode with output enabled, and the NCO is reconnected to the NCO output pin.

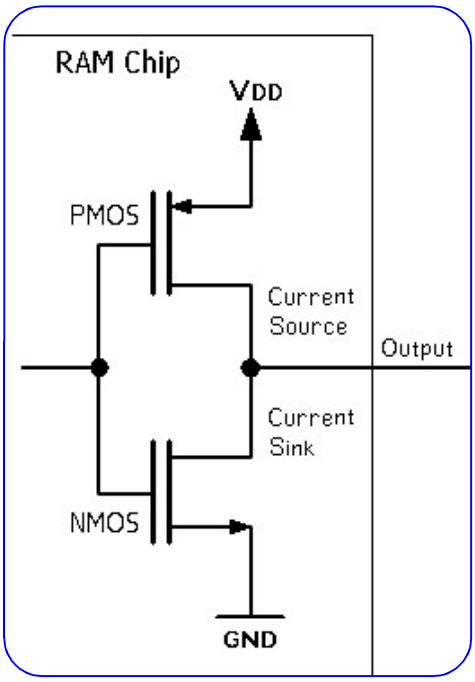


Figure 2.1

Converting the Output RAM's byte wide output to an analog signal requires a digital-to-analog-converter, or DAC. Because the FGEN1 goes to 20 kHz with 256 phase values per cycle, the DAC needs to operate at 5.12 MHz. Finding an inexpensive high-speed single-supply 8-bit DAC in a DIP package was difficult. The few parts available all used current switches feeding an R-2R network. R-2R networks are fast, reliable and inexpensive; see: https://www.electronics-tutorials.ws/combination/r-2r-dac.html. As it turns out, the CMOS outputs of a 6116 static RAM make decent current switches; see Figure 2.1. In fact, the current switches don't need to be perfect, going from 5V to 0V, as long as all eight span the same range. Thus, it is possible to use the 6116's outputs as inputs to the R-2R DAC network. The R-2R network is realized as a thick-film resistor network in a 10-pin SIP. The R-2R network feeds inverting amplifier U8.1 which is offset to analog ground - one-half of the +5 volt analog supply.

2.4 Filter Bank

Schematic sheet 3 shows the filter bank circuitry. The block diagram (Fig. 2.0) shows the relation of the filter bank to the rest of the FGEN circuitry. Appendix G shows the internal functions of the filter bank and the design specifications of the filters.

Any DAC output requires some lowpass filtering to remove its "stair step" output. Some waveforms can be heavily filtered because the waveform itself has low harmonic content - such as a sine wave. Other waveforms - such as a sawtooth wave - have high order harmonics that, if filtered out, would distort the desired waveform. To accommodate different filtering requirements, the FGEN has six second-order Bessel lowpass filters that ratio metrically span the FGEN's output range, these are Filter Banks 0-5. The signal from the waveform generation circuitry feeds a six Filter Banks in parallel. The outputs of Filter Banks 0-5 go to inputs 0-5, respectively, of the 74HC4051 (U9), 8:1 analog multiplexor. The last two inputs to the analog MUX are the unfiltered waveform, on input 6, and analog ground on input 7.

There is a single order lowpass filter (U8.3), known as the Common Filter, on the output of the analog MUX.

There are three different quad op-amps used in the Filter Banks and other analog circuitry. To reduce costs, the gain-bandwidth-product (GBP) of the op-amps was matched to the bandwidth requirements of the circuitry. The MCP6004 (U6) is used for DC voltages and the lowest frequency Filter Bank. The MCP604 (U7) is used for the middle frequency Filter Banks. The MCP6024 (U8) is used for the highest frequency Filter Bank and all op-amps through which the waveform signal

must pass.

Op-amp type	Schematic designation	Gain-Bandwidth-Product (GBP)
MCP6004	U6	1 MHz
MCP604	U7	2.8 MHz
MCP6024	U8	10 MHz

2.5 Gain and Offset

The Gain and Offset circuitry is shown on sheet 4 of the schematics. These controls should both be 10k potentiometers on the front panel, see Appendices B and C for details. These can be single-turn or multi-turn potentiometers. Section 6 has details on how the potentiometers should be connected to the FGEN circuit board. The Gain potentiometer should vary the gain from 0.85 to 2.0. The Offset potentiometer should vary the offset ±0.83 volts. With Gain and Offset it is possible to drive the output waveform's peaks or valleys to the +5V or Ground rails respectively. Therefore, one should always monitor the output waveform to ensure it does not become clipped.

2.6 Front Panel Switches

There are four switches on the front panel; two toggle switches and two pushbuttons. See Appendices B and C for details. Section 6 has details on how the switches should be connected to the FGEN circuit board.

2.7 LCD interface

Liquid Crystal Display (LCD) modules compatible with the FGEN1 circuit board are shown in Appendix B. These two-line by 16-character LCD modules have a 4/8-bit parallel interface with 4 control lines. The FGEN uses the 4-bit parallel interface and treats the LCD module as a write-only device; this allows the LCD to be controlled with only seven I/O pins. Section 6 has details on how the LCD should be connected to the FGEN circuit board.

The contrast of the LCD is controlled by potentiometer VR1. The LCD module is illuminated by LED back-lights. Resistor R29 limits the current to the LED back-lights.

2.8 Host Serial Connector

The RS-232 serial port connector (J4 on schematic sheet 4) is described in detail in Appendix D. U40 is a MAX232A, 5V-powered RS-232 interface with two drivers and two receivers. One receiver/driver pair handles RS-232 data to/from the FGEN1. The other receiver/driver pair receives RTS and sends it back to the host as CTS. RTS is also routed to the RC0 input on the PIC.

3.0 Software Description

3.1 Assembler source code

The assembly language code for the standard Digital Function Generator is programmed into the PIC16F18875 included with the kit. The assembly source code is available upon request. The source code is well commented and highly modular. If you know PIC assembly language it should be easy to understand. If you want to learn more about PIC programming and the free Microchip Assembler (MPASM) consult some of the excellent resources on the Microchip web site.

3.2 Interrupts

No interrupts are used.

3.3 Subroutines

The subroutines are divided into six groups.

1) General Subroutines, such as data conversion; hex to ascii, ascii to hex, delays, etc.
2) UART Subroutines, such as setting baud rates, transmitting and receiving bytes, etc.
3) Synchronous Serial Port Subroutines handle the low level SPI data exchanges.
4) 32-bit Math Subroutines provide 32-bit add, subtract, binary to BCD, and BCD to binary.
5) LCD Module Interface Subroutines format data for display.
6) Function Generator Data Manipulation Subroutines parse ASCII input strings from the host, keep NCO increment values within valid ranges, and swap waveform data locations.

3.4 Main Program

At power up, the PIC initializes all the on-chip peripherals. It then reads waveform 00 from the **EEPROM** into **PIC RAM**, copies the **PIC RAM** to the **Output RAM**, and enables the NCO output. The output waveform will then continue without further action by the PIC. The LED on the PCB will blink eight times and the LCD will display the firmware version programmed in the PIC.

The FGEN then enters Manual Mode. It monitors the front panel switches and RTS every 50 milliseconds. If a front panel switch changes the PIC adjusts the LCD and NCO frequency or waveform accordingly. If RTS goes active the program will jump to Host Mode.

In Host Mode the FGEN sends a menu of options to the Host. Section 4 goes into detail on how these options function. Front panel switches are not functional in Host Mode; however, the Gain and Offset controls still work.

3.5 Firmware modifications

Modification of the Digital Function Generator firmware should only be attempted by someone who is an expert in PIC assembly language programming and possesses a PIC programmer. That being said, for the knowledgeable, the source code provides well documented subroutines and examples from which to learn. An easy way to try out new routines is to activate the debug option on the host communications menu. The debug option in the menu and the jump to the debug option routine are simply “commented out” in the source code.

4.0 Operation

When power is applied to the Digital Function Generator the LED on the circuit board will blink eight times. While the LED is blinking, the LCD display will show “LUCID TECH. Ver. YYYY.MM.DD"; where YYYY.MM.DD is the date of the firmware version programmed in the PIC. After four seconds the display will change to the normal display. The waveform stored at location 00 in the **EEPROM** will be placed in the **Output RAM,** and the frequency will be set to 1000 Hz. Assuming a sine wave is stored at 00, the LCD screen should appear as follows:

```
00 SINE
FREQ 01000.0 Hz
```

4.1 Manual Mode Operation

The two toggle switches and two pushbuttons are active in Manual Mode. The Line toggle switch will move the cursor between the waveform number on the top line and the frequency value on the bottom line. With the cursor on the waveform number, pressing the Increment pushbutton will change the waveform to the next one available in the **EEPROM**. With the cursor on one of the digits in the frequency value on the bottom line, pressing the Increment pushbutton will increase that digit by one. Incrementing a 9 will change the digit to 0 without affecting any other digit. Pressing the Advance pushbutton will move the cursor one digit to the right. Advance will skip over the decimal point and will jump from the tenths of Hz digit to the ten thousand Hz digit. These three switches (Line, Advance and Increment) allow you to select the desired waveform and frequency.

When active, the Filter Bypass toggle switch tells the PIC to keep the analog MUX set to input 6 which means the Common Filter is the only filter in the signal path for any waveform frequency setting. See Appendix G for further information on filtering.

4.2 Host Mode

Host communication mode is entered by connecting an RS-232 cable between FGEN-J4 and the COM port of a host computer. A terminal program must be operating on the host for communication with the FGEN (see Appendix E). The FGEN’s RS-232 connection operates at 9600 baud. The FGEN sends the menu screen:

```
  Lucid Technologies
 FUNCTION GENERATOR 1
 Firmware 2023.01.18

[L]ist waveforms in EEPROM
[U]pload waveform to PIC RAM
[C]opy PIC RAM waveform to output RAM
[S]tore PIC RAM waveform in EEPROM
[D]uplicate EEPROM waveform in PIC RAM
[E]rase waveform from EEPROM
[F]requency
[A]nalog mux
[X] Disconnect from host
[I]nitialize EEPROM chip
 ? _
```

Menu options are selected by typing the corresponding single character, any other entry will be ignored and the menu will be displayed again.

[L]ist waveforms in EEPROM

This option will list the waveforms stored in the **EEPROM** as shown below. # is the waveform number in the **EEPROM**. The waveform number - which determines the storage location in **EEPROM** - is how all waveforms are referenced. Name is the name that will be displayed on the LCD, Date is the date of creation in the waveform file, and Filter is the filter option in the waveform file.

```
? L
 #  Name              Date       Filter
00 SINE              2022-08-27  1
01 SQUARE            2022-08-27  2
02 TRIANGLE          2022-08-27  1
03 +SAWTOOTH         2022-08-27  2
04 -SAWTOOTH         2022-08-27  2
10 SINE^2            2022-08-30  1
11 ECG               2022-08-30  1
```

[U]pload waveform to PIC RAM

This option allows you to upload a waveform file to the **PIC RAM**. Pressing ESCape before the upload begins will abort the option and return you to the menu. See Appendix F for details on the format of waveform files.

```
? U
 Press ESCape to abort.
 Begin text file transfer now.
```

[C]opy PIC RAM waveform to output RAM

This option will copy the waveform from the **PIC RAM** to the **output RAM**. The waveform file will remain in the **PIC RAM** following the copy. To test an experimental waveform file first Upload it to **PIC RAM** then Copy it to **output RAM**.

```
? C
 ERROR - NO WAVEFORM IN RAM BUFFER!
```
(If **PIC RAM** is empty)

or

```
 Done.
```
(If waveform file in **PIC RAM**)

[S]tore PIC RAM waveform in EEPROM

This option will write the waveform file currently in **PIC RAM** into the desired location (waveform number) in **EEPROM**. Pressing escape before the write begins will abort the option and return you to the menu. The waveform file will remain in the **PIC RAM** following the write to the **EEPROM**. This option will overwrite a file already stored in EEPROM with the same waveform

number. To place a new waveform in the EEPROM, List the files to find the waveform number you want to use, Upload the waveform to **PIC RAM,** then Store it in the **EEPROM**.

```
 ? S
 ERROR - NO WAVEFORM IN RAM BUFFER!        (If PIC RAM is empty)
```
or
```
 Press ESCAPE to abort.                    (If waveform file in PIC RAM)
 Enter waveform number (0-13) =
```

[D]uplicate EEPROM waveform in PIC RAM

This option copies a waveform file from the **EEPROM** to the **PIC RAM**. "Duplicate" was used because Copy was already taken for another option. Pressing ESCAPE before the copy begins will abort the option and return you to the menu. While in Host Mode, to output a waveform stored in the **EEPROM** you must Duplicate it from **EEPROM** to **PIC RAM**, then Copy it from **PIC RAM** to **output RAM**.

```
? D
 Press ESCAPE to abort.
 Enter waveform number (0-13) =
```

[E]rase waveform from EEPROM

This option erases a waveform file stored in the **EEPROM.** Pressing ESCAPE before the erase begins will abort the option and return you to the menu. Any waveform file in the **PIC RAM** will be deleted by this option. Erase will erase any data at the desired waveform number, even if there was no file there to begin with.

```
? E
 Press ESCAPE to abort.
 Enter waveform number (0-13) =
```

[F]requency

This option will change the frequency of the output waveform. Pressing ESCAPE before the frequency is changed will abort the option and return you to the menu. The desired frequency should be entered in Hertz. Following are acceptable ways to input 100 Hz:

100
0100
100.0

Any entry beyond the frequency range of the FGEN will be limited to maximum (20000 Hz) or minimum (0.1 Hz) as appropriate. The analog MUX setting is not changed by this option.

```
? F
Press ESCAPE to abort.
 Enter frequency in Hz =
```

[A]nalog MUX

This option will change the setting of the analog MUX. Pressing ESCAPE before the MUX is changed will abort the option and return you to the menu. MUX settings of 0 through 7 are possible. See Appendix G for details.

```
? A
Press ESCAPE to abort.
Enter MUX channel (0-7) =
```

[I]nitialize EEPROM chip

This option will set all bytes in the **EEPROM** to zero. Pressing ESCAPE before the erase will abort the option and return you to the menu.

```
 ? I
 This option will initialize the EEPROM chip.
 This will erase all stored waveforms.
 Press Y to proceed.
 Press ESCAPE to abort.
```

[X] Disconnect from host

This option ***must*** be selected before terminating Host Mode. If the RS-232 connection is removed before selecting this option the FGEN will be caught in a loop waiting for a menu selection. If this happens, restarting the FGEN will return it to normal operation.

```
? X
 Remove RS-232 cable.
```

5.0 FGEN Circuit Board Assembly

5.1 Preparation

You will need the following tools:

> A low wattage soldering pencil, approximately 10 to 20 Watts.
> Flux core solder wire, organic flux core preferred.
> Lead benders.
> Lead/wire clippers.

Before beginning assemble, carefully check the FGEN circuit board for shorted or incomplete traces and confirm all parts against the list in Appendix A.

5.2 Assembly checklist

Check the value/type of each part as you assemble the board. Check off each item as you proceed through the checklist. The 1% resistors and C22 are already soldered. Clip excess lead length from each component after it's soldered. See Appendix H for parts placement.

Insert and solder the low-profile sockets for:

____ U1 40-pin DIP
____ U2 8-pin DIP
____ U3 16-pin DIP
____ U4 20-pin DIP
____ U5 24-pin DIP
____ U6 14-pin DIP
____ U7 14-pin DIP
____ U8 14-pin DIP
____ U9 16-pin DIP
____ U40 16-pin DIP
____ Y1 XP-8 oscillator socket

Do NOT insert the chips in the sockets yet!

Insert and solder the following components.

____ R1 4.7K, 0.25W, 5% (yellow-violet-red-gold)
__x_ R2 33K, 0.25W, 1% (orange-orange-black-red-brown)
__x_ R3 33K, 0.25W, 1% (orange-orange-black-red-brown)
__x_ R4 5.6K, 0.25W, 1% (green-blue-black-brown-brown)
__x_ R5 28.7K, 0.25W, 1% (red-grey-violet-red-brown)
__x_ R6 53.6K, 0.25W, 1% (green-orange-blue-red-brown)
__x_ R7 5.6K, 0.25W, 1% (green-blue-black-brown-brown)
__x_ R8 10K, 0.25W, 1% (brown-black-black-red-brown)
__x_ R9 2.0K, 0.25W, 1% (red-black-black-brown-brown)
__x_ R10 4.12K, 0.25W, 1% (yellow-brown-red-brown-brown)
__x_ R11 5.36K, 0.25W, 1% (green-orange-blue-brown-brown)
__x_ R12 10K, 0.25W, 1% (brown-black-black-red-brown)
__x_ R13 12K, 0.25W, 1% (brown-red-black-red-brown)

__x_	R14	25.5K, 0.25W, 1%	(red-green-green-red-brown)
__x_	R15	7.5K, 0.25W, 1%	(violet-green-black-brown-brown)
__x_	R16	13.3K, 0.25W, 1%	(brown-orange-orange-red-brown)
__x_	R17	8.66K, 0.25W, 1%	(grey-blue-blue-brown-brown)
__x_	R18	10K, 0.25W, 1%	(brown-black-black-red-brown)
__x_	R19	10K, 0.25W, 1%	(brown-black-black-red-brown)
__x_	R20	15K, 0.25W, 1%	(brown-green-black-red-brown)
__x_	R21	7.5K, 0.25W, 1%	(violet-green-black-brown-brown)
__x_	R22	15K, 0.25W, 1%	(brown-green-black-red-brown)
____	R23	6.8K, 0.25W, 5%	(blue-grey-red-gold)
____	R24	10K, 0.25W, 5%	(brown-black-orange-gold)
____	R25	10K, 0.25W, 5%	(brown-black-orange-gold)
____	R26	10K, 0.25W, 5%	(brown-black-orange-gold)
____	R27	10K, 0.25W, 5%	(brown-black-orange-gold)
____	R28	470 ohm, 0.25W, 5%	(yellow-violet-red-gold)
____	R29	82 ohm, 0.5W, 5%	(grey-red-black-gold)
____	R30	5k, trim pot	
____	R40	1.1K, 0.25W, 5%	(brown-brown-red-gold)
____	R41	1.1K, 0.25W, 5%	(brown-brown-red-gold)
____	RN1	10-pin SIP, pin 1 goes in the square pad	

____	C1	0.1 uFd, radial, 0.1" lead spacing
____	C2	0.1 uFd, radial, 0.1" lead spacing
____	C3	100 uFd, axial, positive lead toward square pad
____	C4	0.1 uFd, radial, 0.1" lead spacing
____	C5	0.15 uFd, radial, 0.1" lead spacing, marked 154
____	C6	0.1 uFd, radial, 0.1" lead spacing
____	C7	0.1 uFd, radial, 0.1" lead spacing
____	C8	0.001 uFd, disk, 0.2" lead spacing
____	C9	1 uFd, radial, 0.2" lead spacing, marked 105
____	C10	0.1 uFd, radial, 0.1" lead spacing
____	C11	0.22 uFd, radial, 0.1" lead spacing, marked 224
____	C12	0.22 uFd, radial, 0.1" lead spacing, marked 224
____	C13	0.1 uFd, radial, 0.1" lead spacing
____	C14	0.15 uFd, radial, 0.1" lead spacing, marked 154
____	C15	0.15 uFd, radial, 0.1" lead spacing, marked 154
____	C16	100 uFd, axial, positive lead toward square pad
____	C17	1 uFd, radial, 0.2" lead spacing, marked 105
____	C18	1 uFd, radial, 0.2" lead spacing, marked 105
____	C19	0.1 uFd, radial, 0.1" lead spacing
____	C20	0.1 uFd, radial, 0.1" lead spacing
____	C21	0.015 uFd, radial, 0.1" lead spacing, marked 153
__x_	C22	0.1 uFd, radial, 0.1" lead spacing, marked 104
____	C23	0.0015 uFd, radial, 0.1" lead spacing, marked 152
____	C24	0.01 uFd, radial, 0.1" lead spacing, marked 103

____ C25 0.001 uFd, radial, 0.1" lead spacing, marked 102
____ C26 1 uFd, radial, 0.2" lead spacing, marked 105
____ C27 100 pFd, radial, 0.1" lead spacing, marked 101
____ C28 470 pFd, radial, 0.1" lead spacing, marked 471
____ C29 680 pFd, radial, 0.1" lead spacing, marked 681
____ C30 0.1 uFd, radial, 0.1" lead spacing
____ C31 0.001 uFd, disk, 0.2" lead spacing
____ C32 0.001 uFd, disk, 0.2" lead spacing
____ C40 1 uFd, radial, 0.2" lead spacing, marked 105
____ C41 1 uFd, radial, 0.2" lead spacing, marked 105
____ C42 1 uFd, radial, 0.2" lead spacing, marked 105
____ C43 1 uFd, radial, 0.2" lead spacing, marked 105
____ C44 0.1 uFd, radial, 0.1" lead spacing

____ LED1 4 mm red LED, the long lead leg is the anode and goes in the round hole
____ J2 +9V DC power jack
____ J4 DB9 female connector

At this point you will need to make some decisions on how you want to connect the various FGEN controls and LCD module. Headers are supplied for connectors with 0.1 inch spacing, but you can solder wires directly to the FGEN circuit board if you prefer. Header SW1 is provided if you want to use an On/Off switch instead of just connecting and disconnection the +9V supply.

____ SW1 1x2 pin header for optional On/Off switch
____ J1 1x3 pin header for Gain potentiometer
____ J3 1x16 pin header for LCD module
____ J5 1x5 pin header for front panel switches
____ J6 1x2 pin header for output signal
____ J7 1x3 pin header for Offset potentiometer

The next assembly step is the voltage regulators (U10, U11) and heatsink. U10 and U11 are both 78M05 regulators so they are interchangeable. The back - metal tab side - of both regulators should touch the heatsink. Use the No. 6 nut and screw to firmly grip the heatsink between the regulator, as shown in Figure 5.1 and H2. Insert the legs of the regulators in the circuit board pads for U10 and U11. The bodies of the regulator chips should be about 0.1" above the board. Solder the regulator legs while ensuring the regulator/heatsink remain vertical and perpendicular to the circuit board.

____ U10 78M05
____ U11 78M05

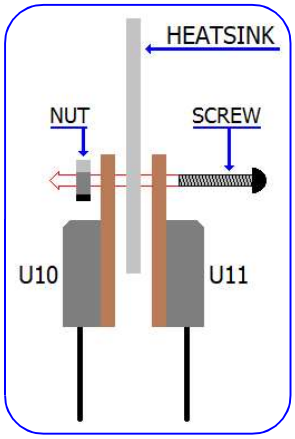


FIGURE 5.1

The last construction step is to clean the board. If you used organic core solder just rinse the board in warm water. If you used acid core solder try scrubbing it with an old toothbrush and rubbing alcohol.

5.3 Circuit Board Checkout

You will need a multimeter to check out the FGEN circuit board. Place the FGEN circuit board on an insulating surface. DO NOT install the integrated circuits yet.

Attach the negative lead of your voltmeter to the ground test point. Plug-in your 9V wall transformer and connect it to J2 on the FGEN. Be sure there is a jumper on SW1. The supply voltage should measure at least 8VDC on the positive lead of C9 (1 uFd) just to the right of J2. Next we will measure the Analog and Digital +5V supplies. These voltages should be between 4.9 and 5.1 volts.

The Digital +5V supply, from U10, should be measured at:

DIGITAL +5V test point
U1 pins 11 and 32
U2 pins 3, 7 and 8
U3 pin 16
U4 pin 20
U5 pin 24
U40 pin 16
J3 pin 2

The Analog +5V supply, from U11, should be measured at:

ANALOG +5V test point
U6 pin 4
U7 pin 4
U8 pin 4
U9 pin 16

If there is a problem, disconnect the wall transformer and inspect the FGEN circuit board. The heatsink may be warm to the touch but should never, even with the chip installed, be too hot to hold. Be sure the polarized capacitors C3 and C16 are not installed backwards. Refer to the schematics and check the value of all other resistors and capacitors. Correct any errors and check +5V again.

After the FGEN +5V supplies checkout, and the wall transformer is disconnected, you can install the integrated circuits or you can wait and install them after connecting all the controls (Section 6). Refer to Appendix A for the reference assigned to each chip and Figure H1 for the location on the circuit board. Be sure to check the position of pin 1 when installing the integrated circuits. Pay particular attention to the orientation of Y1 which, because of its symmetry, could be installed in four different orientations; see Figure H2 for the correct orientation.

6.0 Installation

6.1 Prepare the Front Panel

Assuming you are using the suggested CM6-300 or 325XP6 case for the Digital Function Generator, the diagram for the front panel is shown in Appendix C. There are eleven holes and one window cutout in the front panel. Figure C3 shows an aluminum front panel but the plastic front panel that comes with the CM6-300 is completely adequate. The items required for the front panel (switches, potentiometers, LCD module and output connector) are listed in Appendix B.

Fit the switches in the front panel. Fit the potentiometers in the front panel. Fit the Output BNC connector in the front panel. Fit the installation of the LCD module. The LCD module should have its connection points at the top, as shown in Figure C4.

6.2 Prepare the Rear Panel

There is no diagram for the rear panel, in fact the rear panel is optional. If you use a rear panel simply notch out rectangles for J2 and J4 along the bottom of the panel.

6.3 Wiring the Front Panel Controls

The point-of-view for diagrams and descriptions in this section is from the rear of the FGEN, as illustrated in Figure C4. Closeup views of the circuit board are in Appendix H.

6.3.1 Gain and Offset Potentiometers

Both potentiometers should be 10 kohms. Either single-turn or multi-turn potentiometers may be used. J1 is the Gain potentiometer while J7 is the offset potentiometer. The connections for both are as shown in Table 6.1. NOTE, however, that J1 has pin 1 on the right while J7 has pin 1 on the left.

Table 6.1

J1 or J7 pin number	Potentiometer connection
1	Clock Wise
2	Wiper
3	Counter Clock Wise

6.3.2 Front Panel Switches

Wire the front panel switches to J5 as shown in Table 6.2. Note that J5 has pin 1 on the right. Pins 1-4 are logic inputs with 10k pullups. Table 6.2 shows logic inputs should be pulled to Ground. Because pin 5 is the only Ground on the connector, it must be connected to all the switches.

Table 6.2

J5 pin number	Switch function	Notes
1	Filter Bypass Toggle	Grounded when switch is in Bypass position
2	Line Select Toggle	Grounded when switch is in up (waveform line)
3	Advance Pushbutton	Grounded when button is depressed
4	Increment Pushbutton	Grounded when button is depressed
5	GROUND	Distributed to all front panel switches.

6.3.3 LCD Module

The LCD module should be mounted so that its connection points are at the top, as shown in Figure C4. J3 is the connector for the LCD module. The LCD module and J3 both have pin 1 on the right. The 16 pins of J3 correspond with the 16 pins on the LCD module. Wire J3 pin1 to LCD pin 1, J3 pin 2 to LCD pin 2, etc. Note that pins 7, 8, 9 and 10 are unused and do not need to be wired. The FGEN interfaces with the LCD module via a 4-bit interface rather than the usual 8-bit interface. Thus, the four data lines on those pins are unused.

6.4 Initial Power Up

There are several things that need to be done to initialize your Digital Function Generator after you plug-in your 9V wall transformer and connect it to J2 on the FGEN.

The 5k trimmer on the FGEN1 circuit board (R30) controls the contract of the LCD module. When power is first applied to the LCD module, the display may be very bright, or all character blocks may be black. Adjust R30 until the text on the display is clearly legible.

When power is applied to the Digital Function Generator the waveform stored at location 00 in the **EEPROM** will be placed in the **Output RAM,** and the frequency will be set to 1000 Hz. However, at initial power up there are no waveforms in the EEPROM and the output will be a constant voltage. You need to store waveforms in the EEPROM which must be done via the RS-232 connection at 9600 baud.

1. Download or create the waveforms you want on your computer, see Appendix F.
2. Power up the FGEN and establish an RS-232 connection, see Appendix E.
3. Select the **[I]nitialize EEPROM chip** option from the Host Mode menu.
4. Select the **[L]ist waveforms in EEPROM** option. No waveforms should be listed.
5. Select the **[U]pload waveform to PIC RAM** option. You will need to start the waveform TXT file transfer from the terminal program on your computer.
6. Select the **[S]tore PIC RAM waveform in EEPROM** option. You will need to specify the waveform number in EEPROM (00-13).
7. Repeat steps 5 and 6 for each new waveform.
8. Select the **[L]ist waveforms in EEPROM** option. You should see the waveforms you stored in EEPROM.
9. Select the **[X] Disconnect from host** option from the Host Mode menu and disconnect the RS-232 cable.
10. Power down and restart the Digital Function Generator.

7.0 Customization

The FGEN circuit board does not need to be installed in the CM6-300 or 325XP6 case suggested by this manual. That case's small front panel limits the number of controls. In a larger case there could room for an AC powered 9V DC power supply with a power switch - wired to SW1 - on the front panel. Configuring the layout of the finished FGEN is entirely up to you.

APPENDIX A

FGEN1 CIRCUIT BOARD PARTS LIST

Quantity	Part	Reference	
11	0.1uF, Bypass, 0.1" LS	C1,C2,C4,C6,C7,C10,C13,C19,C20,C30,C44	
2	100uF, Electrolytic, axial	C3,C16	
3	0.15 uF, Ceramic, 0.1" LS	C5,C14,C15	
3	0.001 uF, Ceramic disk, 0.2" LS	C8,C31,C32	
8	1.0uF, Ceramic, 0.2" LS	C9,C17,C18,C26,C40,C41,C42, C43	
2	0.22 uF, Ceramic, 0.1" LS	C11,C12	
1	0.015 uF, Ceramic, 0.1" LS	C21	
1	0.1 uF, Ceramic, 0.1" LS	C22	
1	0.0015 uF, Ceramic, 0.1" LS	C23	
1	0.01 uF, Ceramic, 0.1" LS	C24	
1	0.001 uF, Ceramic, 0.1" LS	C25	
1	100 pF, Ceramic, 0.1" LS	C27	
1	470 pF, Ceramic, 0.1" LS	C28	
1	680 pF, Ceramic, 0.1" LS	C29	
1	4.7K, 0.25W, 5%	R1	(yellow-violet-red-gold)
2	33K, 0.25W, 1%	R2,R3	
2	5.6K, 0.25W, 1%	R4,R7	
1	28.7K, 0.25W, 1%	R5	
1	53.6K, 0.25W, 1%	R6	
4	10.0K, 0.25W, 1%	R8,R12,R18,R19	
1	2.0K, 0.25W, 1%	R9	
1	4.12K, 0.25W, 1%	R10	
1	5.36K, 0.25W, 1%	R11	
1	12.0K, 0.25W, 1%	R13	
1	25.5K, 0.25W, 1%	R14	
2	7.5K 0.25W, 1%	R15,R21	
1	13.3K, 0.25W, 1%	R16	
1	8.66K, 0.25W, 1%	R17	
2	15.0K, 0.25W, 1%	R20, R22	
1	6.8K, 0.25W, 5%	R23	(blue-gray-red-gold)
4	10K, 0.25W, 5%	R24,R25,R26,R27	(brown-black-orange-gold)
1	470, 0.25W, 5%	R28	(yellow-violet-brown-gold)
1	82, 0.5W, 5%	R29	(gray-red-black-gold)
1	5K trim pot	R30	
2	1.1K, 0.25W, 5%	R40,R41	(brown-brown-red-gold)
1	R/2R network, 4610X-R2R	RN1	

Quan.	Part	Reference
1	PIC16F18875-I/P, 40-DIP	U1
1	25LC230, 8-DIP	U2
1	74HC4040, 16-DIP	U3
1	74HC573, 20-DIP	U4
1	6116, 24-DIP	U5
1	MCP6004-I/P, 14-DIP	U6
1	MCP604-I/P, 14-DIP	U7
1	MCP6024-I/P, 14-DIP	U8
1	74HC4051, 16-DIP	U9
2	78M05CP, TO-220	U10,U11
1	MAX232ACPE, 16-DIP	U40
1	26.8435 MHz oscillator, XO-8	Y1
1	40-DIP (0.6") socket	U1
1	8-DIP socket	U2
3	16-DIP socket	U3,U9,U40
1	20-DIP socket	U4
1	24-DIP (0.6") socket	U5
3	14-DIP socket	U6,U7,U8
1	XO-8 socket	Y1
1	4mm red LED	LED1
2	1x3 potentiometer headers	J1,J7
1	DC power jack	J2
1	1x16 LCD module header	J3
1	DB9 female connector	J4
1	1x5 switch inputs header	J5
1	1x2 BNC output header	J6
1	1x2 header for power	SW1
1	FGEN1 circuit board	
1	Jumper for SW1	
1	Aluminum heat sink	
1	#6 nut and screw to connect U10, U11 and heatsink	
4	PCB mounting screws	

APPENDIX B

USER SUPPLIED PARTS

The FGEN1 kit sold by Lucid Technologies only includes the parts needed to assemble the circuit board, those shown in Appendix A; it does not include all the parts necessary for a operable Function Generator. Lucid Technologies suggests the case, switches, display and other parts listed here. Where acceptable parts are known, part numbers are shown. Equivalent parts may be available from other sources.

Plastic case, 1 required

PacTec Enclosures	www.pactecenclosures.com	610-361-4200
	Part# CM6-300	
Simco	www.simcobox.com	863-452-9090
	Part# 325XP6	

Toggle switches, miniature, SPST, Off-On, 2 required for Pulse/Square and Line Select switches

Jameco Electronics	www.jameco.com	800-831-4242
	Part# 76523	

Pushbutton switches, snap-action, miniature, momentary, Normally Open, 2 required for Digit Advance and Digit Increment switches

Jameco Electronics	www.jameco.com	800-831-4242
	Part# 596799	

Gain and Offset potentiometers, 10 k, linear taper, two required.

BNC connector, 50 ohm, bulkhead, 1 required (output), 1 optional (clock out)

Jameco Electronics	www.jameco.com	800-831-4242
	Part# 71590	

Wall transformer, 9VDC, 100 mA or more, coaxial power plug, 5.5mm O.D., 2.1mm I.D., center positive, 1 required

Jameco Electronics	www.jameco.com	800-831-4242
	Part# 100845	
Mouser Electronics	www.mouser.com	800-346-6873
	Part# 553-WDU9-100	

LCD display module, 80 x 36 mm, 2 lines of 16 characters, 5 VDC operation, backlight, 1 required.

Jameco Electronics	www.jameco.com	800-831-4242
	Part# 2333231, 2295423	
Elecrow	www.elecrow.com	
	Part# DLC01602B	

LCD mounting hardware. Four each of:

#4-40 x 5/8" (16 mm) pan head machine screws
#4-40 machine screw nuts
#4 standoffs, 0.3" (7.6 mm)

APPENDIX C

CHASSIS DETAILS

The following drawings and pictures are based on the recommended CM6-300 case. The picture shows an aluminum front panel but the plastic panel that comes with the CM6-300 works just fine.

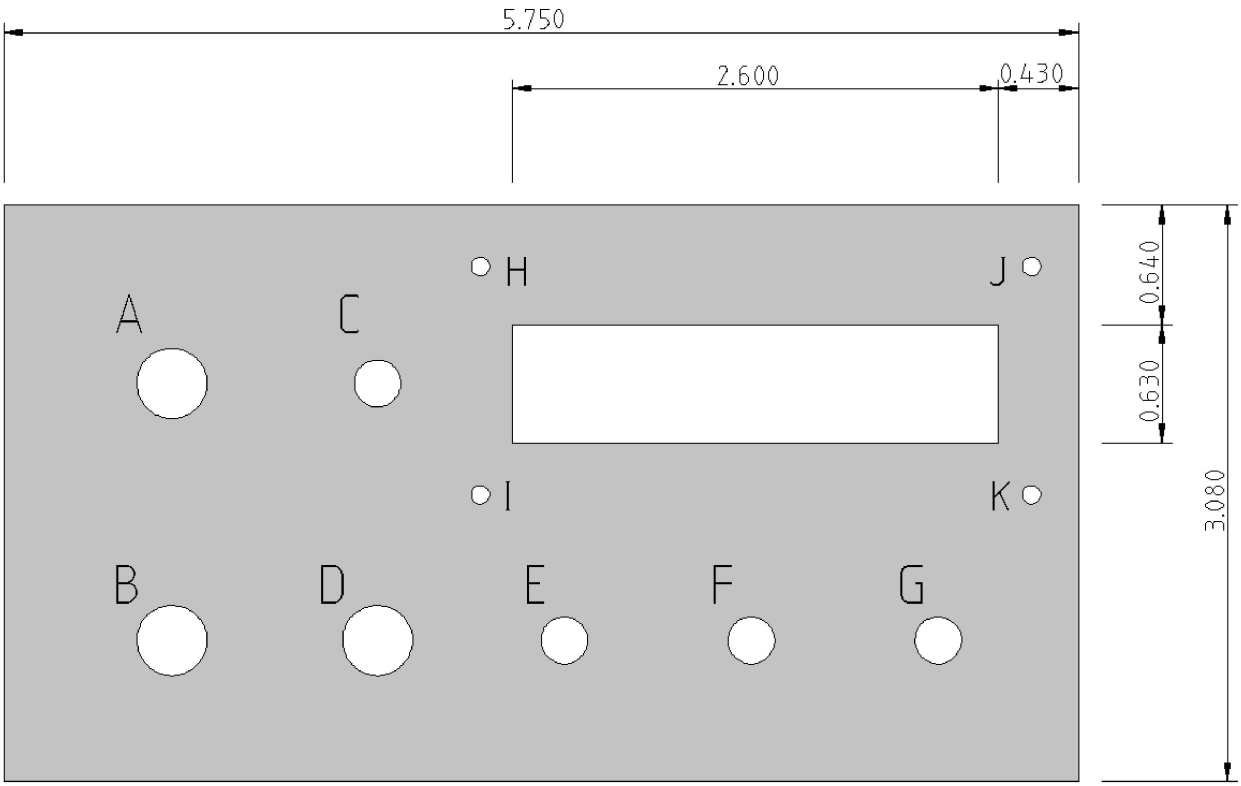


Figure C1. Front panel layout and dimensions (inches).

Front panel thickness is 0.062 inches (1.6 mm).

The LCD display module should be mounted with the connection pins at the top.

Table C1. Coordinates and diameter of front panel holes. All dimensions are in inches. Origin (0,0) is at the lower-left of the diagram, Figure C1.

Key	Description	X	Y	Diameter
A	Offset control	0.900	2.125	0.375
B	Gain control	0.900	0.750	0.375
C	Line selection switch	2.000	2.125	0.250
D	Output BNC	2.000	0.750	0.375
E	Filter bypass switch	3.000	0.750	0.250
F	Advance cursor pushbutton	4.000	0.750	0.250
G	Increment digit pushbutton	5.000	0.750	0.250
H	LCD mount, upper-left, #4 screw	2.550	2.750	0.125
I	LCD mount, lower-left, #4 screw	2.550	1.530	0.125
J	LCD mount, upper-right, #4 screw	5.500	2.750	0.125
K	LCD mount, lower-right, #4 screw	5.500	1.530	0.125

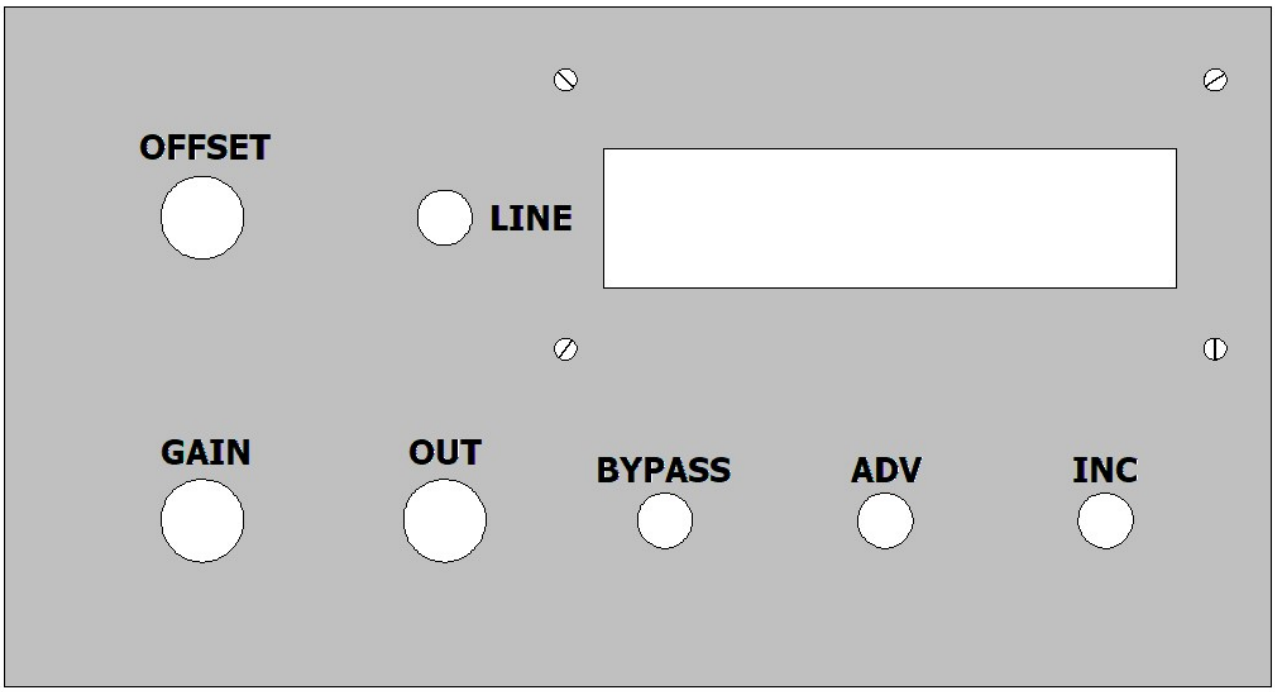


Figure C2. Front panel labels.

Figure C3. Finished front panel.

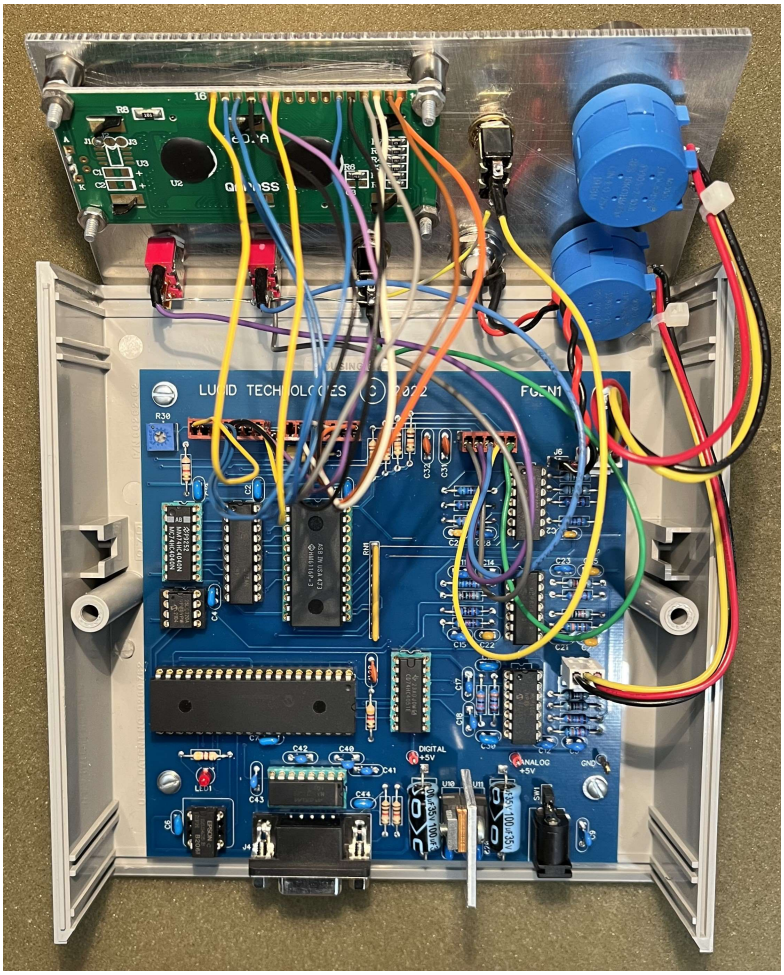


Figure C4. Circuit board and front panel assembly.

APPENDIX D

RS-232 SERIAL INTERFACE CONNECTOR

The table below shows the most commonly implemented signals and their pin assignments in accordance with RS-232D. Host computers are usually DTE (Data Terminal Equipment) and modems are DCE (Data Communications Equipment). Note that circuits are named from the point of view of the DTE. For example, circuit BB (receive data) is actually data transmitted by the DCE. DCE devices originally used a 25 pin, female, D connector.

Pin	Circuit	Description	Direction
1	AA	Protective ground, PG	n/a
2	BA	Transmit data, TD	to DCE
3	BB	Receive data, RD	from DCE
4	CA	Request to send, RTS	to DCE
5	CB	Clear to send, CTS	from DCE
6	CC	Data set ready, DSR	from DCE
7	AB	Signal ground, SG	n/a
8	CF	Data carrier detect, DCD	from DCE
20	CD	Data Terminal ready, DTR	to DCE
22	CE	Ring indicator, RI	from DCE

In recent years all personal computer have migrated to the use of a 9 pin, male, D connector instead of the 25 pin connector. The pin assignments for such a DTE device are shown below.

Pin	Circuit	Description	Direction
1	CF	Data carrier detect, DCD	from DCE
2	BB	Receive data, RD	from DCE
3	BA	Transmit data, TD	to DCE
4	CD	Data Terminal ready, DTR	to DCE
5	AB	Signal ground, SG	n/a
6	CC	Data set ready, DSR	from DCE
7	CA	Request to send, RTS	to DCE
8	CB	Clear to send, CTS	from DCE
9	CE	Ring indicator, RI	from DCE

All Lucid Technologies products are designed as DCE devices. They use a 9 pin, female, D connector that is directly compatible with 9 pin COM ports found on personal computers. The pin assignments for this connector are shown below.

Pin	Circuit	Description	Direction
1	CF	Data carrier detect, DCD	from Digital Pulse Generator
2	BB	Receive data, RD	from Digital Pulse Generator
3	BA	Transmit data, TD	to Digital Pulse Generator
4	CD	Data Terminal ready, DTR	to Digital Pulse Generator
5	AB	Signal ground, SG	n/a
6	CC	Data set ready, DSR	from Digital Pulse Generator
7	CA	Request to send, RTS	to Digital Pulse Generator
8	CB	Clear to send, CTS	from Digital Pulse Generator
9	CE	Ring indicator, RI	from Digital Pulse Generator

None of the handshake lines are actively controlled by the Digital Pulse Generator. DTR is not connected and thus is ignored. DSR and DCD are hard-wired to the ON condition (ON = spacing = +voltage) at all times. RTS is received, buffered, and looped back to the host as CTS; thus CTS tracks RTS.

APPENDIX E

RS-232 COMMUNICATIONS SETUP

New PCs may not possess a COM port but serial communication is still possible via a USB-to-Serial-Adapter.

Your host computer must run a terminal emulation program to communicate with the FGEN. Several freeware terminal emulation programs are available. We will use HyperTerminal here as an example because it came bundled with early versions of Microsoft Windows and is still popular. Free terminal emulators, such as ZOC Terminal or Tera Term, will also work.

When you first start HyperTerminal a Connection_Description window will come up. Enter a name, such as “FGEN", and select an icon, then click OK. A Connect_To window will come up. Go to the Connect_Using line and select the COM-port you will use to connect to the Digital Pulse Generator; then click OK. Remember, this is a direct connection, you are not going through a modem. A COMX_Properties window will come up next. Make the following settings:

Data bits = 8
Parity = None
Stop bits = 1
Flow control = None, then click OK.
Select 9600 baud.

Now click on the File menu, Properties, and select the Settings tab. Set Emulation to ANSI. Click on the ASCII_Setup button. Set the Line_delay to 1 millisecond and the Character_delay to 0 milliseconds. Click the OK button for the ASCII_setup window and the OK button on the Properties window.

The last step in the setup is to save the terminal settings so you won't have to go through this process every time you use HyperTerminal. Click on the File menu, Save_as, check that the file name is correct, (for example FGEN.ht) and click on Save. The next time you want to run HyperTerminal you can simply double-click on the file name (FGEN.ht) and HyperTerminal will begin with all the correct settings.

Turn on your FGEN and connect the COM-port. When the FGEN detects RTS from the Host (your PC) it will switch to the Host Mode.

APPENDIX F

Waveform File Format

Waveform files are straight ASCII text files that may be created with Notepad or a similar editor. Several common waveform files are available for download at https://www.lucidtechnologies.info/docs.htm. Waveform files should use a TXT file extension. Line Feed (LF = 0x0A) and Carriage Return (CR = 0x0D) are ignored, other ASCII control characters (<= 0x1F) in the file will cause an error. There are five fields in a waveform file, one is optional and four are required. The fields must appear in the specified order. The four required fields must all begin with an ASCII Asterisk "*" (0x2A). An example file is shown at the end of this appendix.

Comment Field

This field is optional. It may contain up to 255 characters. It does not begin with, nor may it contain, an asterisk.

Name Field

This field is required and must begin with an asterisk. This is the name that will be displayed by the FGEN, it must be less than 16 characters.

Date Field

This field is required and must begin with an asterisk. These ten bytes are the year-month-day; YYYY-MM-DD.

Filter Field

This field is required and must begin with an asterisk. This single character specifies the filtering used for the waveform. See Appendix G for details on filtering schemes.

Data Field

This field is required and must begin with an asterisk. This field lists the 256 byte values in one cycle of the waveform. The 8-bit Analog ground is approximately 0x7F. Values greater than analog ground are 0x80-0xFF, while values less than analog ground are 0x00-0x7E. Each byte is stored in ASCII-HEX format as two ASCII characters without the leading “0x”. Thus 0x7F is simply 7F.

This field must contain 512 ASCII characters representing the 256 bytes in one cycle of the waveform. Valid characters are 0-9, A-F and a-f. For example, 0xA7 will be sent as the two ASCII bytes, "A" (0x41) and "7" (0x37). The two ASCII characters representing one byte may not be split between lines. The data field must be terminated by an ASCII Percent "%" (0x25) character.

Contents of the file “SINE_2022-08-30.txt”.

```
Sine wave file created by Brian Beard
*SINE
*2022-08-30
*1
*
7F8286898C8F9295989B9EA1A4A7AAAD
B0B3B6B8BBBEC1C3C6C8CBCDD0D2D5D7
D9DBDDDFE1E3E5E7E9EAECEEEFF1F2F3
F4F6F7F8F9FAFAFBFCFCFDFDFEFEFEFE
FEFEFEFEFEFDFDFCFCFBFAFAF9F8F7F6
F4F3F2F1EFEEECEAE9E7E5E3E1DFDDDB
D9D7D5D2D0CDCBC8C6C3C1BEBBB8B6B3
B0ADAAA7A4A19E9B9895928F8C898682
7F7C797673706D6A6764615E5B585552
4F4C494644413E3C393634312F2D2A28
2624211F1D1B1A1816141311100E0D0B
0A0908070605040403020202010101010
0101010101020202030404050607080 9
0A0B0D0E1011131416181A1B1D1F2124
26282A2D2F313436393C3E414446494C
4F5255585B5E6164676A6D707376797C
%
```

APPENDIX G

FILTER BANK SPECIFICATIONS

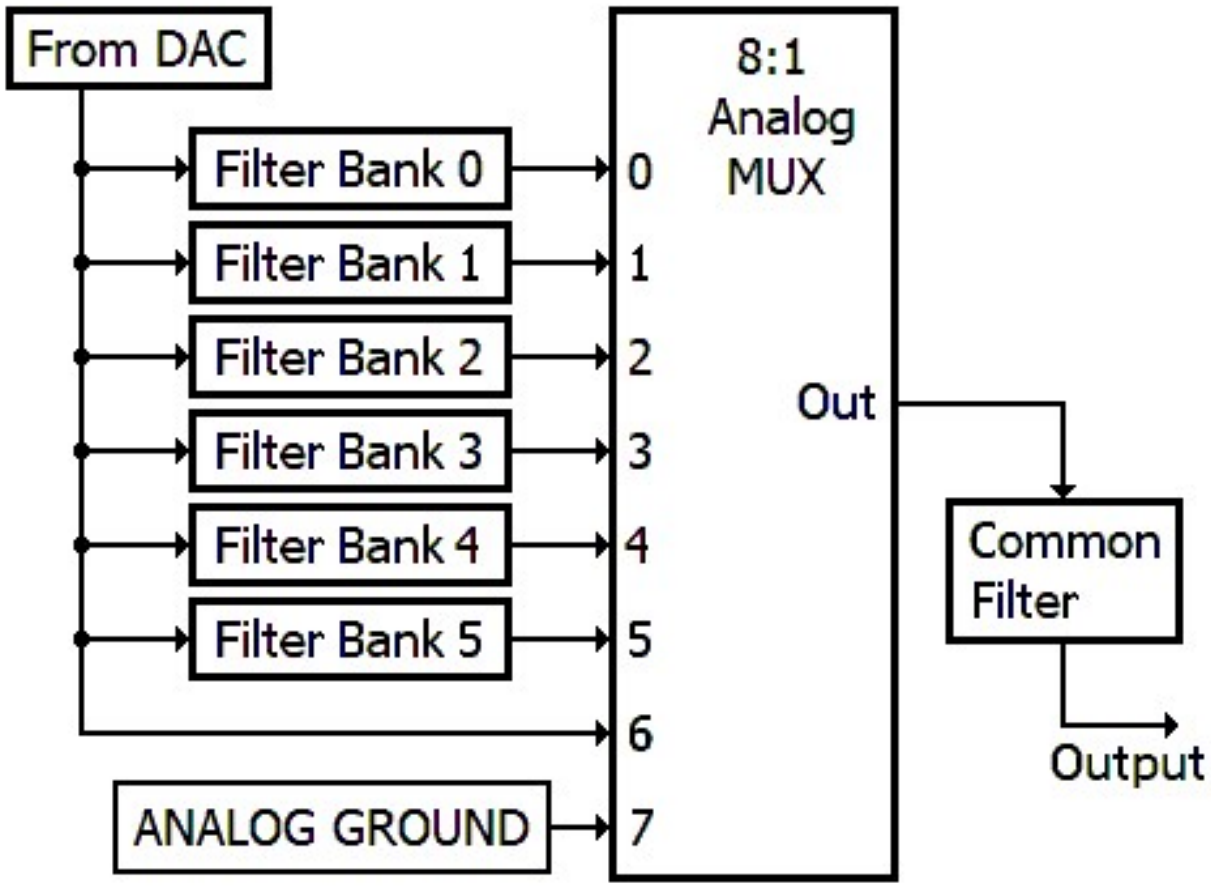


Figure G1. Filter Bank diagram

As shown in Figure G1 above, the Filter Bank consists of seven filters and an Analog MUX. Filter Banks 0-5 are unity-gain second-order Bessel low-pass-filters. The Common Filter is a unity-gain first-order Bessel low-pass filter. The specifications of the filters are shown in Table G1. The signal passed through the Analog MUX to the Common Filter is determined by three digital port outputs from the CPU. Note that the waveform signal always passes through the Common Filter, hence the name! So, even when the Filter Bypass switch is on, the Common Filter is still in the signal path. During normal operation, the CPU will select the proper MUX channel based on the filter field in the waveform file and the frequency. Table G2 summarizes this function. Consider a Filter Field value of 5; for an output at 10 Hz the waveform would pass through Filter Bank 5 and the Common filter, for frequencies greater than 16 Hz only the Common filter would be in the signal path.

Table G1. Filter specifications.

Filter Bank	Filter order	-3 dB cutoff	Step function rise time
0	2	17.6 Hz	19.9 msec
1	2	88 Hz	3.9 msec
2	2	352 Hz	0.99 msec
3	2	1408 Hz	0.25 msec
4	2	5632 Hz	62 µsec
5	2	22 kHz	16 µsec
Common	1	183 kHz	1.9 µsec

Table G2. Filter Bank selection as a function of filter option and output frequency

Waveform Filter Field	0.1 - 16 Hz	16.1 - 80 Hz	80.1 - 320 Hz	320.1 - 1280 Hz	1280.1 - 5120 Hz	5120.1 - 20000 Hz
0	0	1	2	3	4	5
1	1	2	3	4	5	Common
2	2	3	4	5	Common	Common
3	3	4	5	Common	Common	Common
4	4	5	Common	Common	Common	Common
5	5	Common	Common	Common	Common	Common
6	Common	Common	Common	Common	Common	Common
7	Ground	Ground	Ground	Ground	Ground	Ground
8	0	0	0	0	0	0
9	1	1	1	1	1	1
A	2	2	2	2	2	2
B	3	3	3	3	3	3
C	4	4	4	4	4	4
D	5	5	5	5	5	5
E	na	na	na	na	na	na
F	na	na	na	na	na	na

APPENDIX H

FGEN1 CIRCUIT BOARD

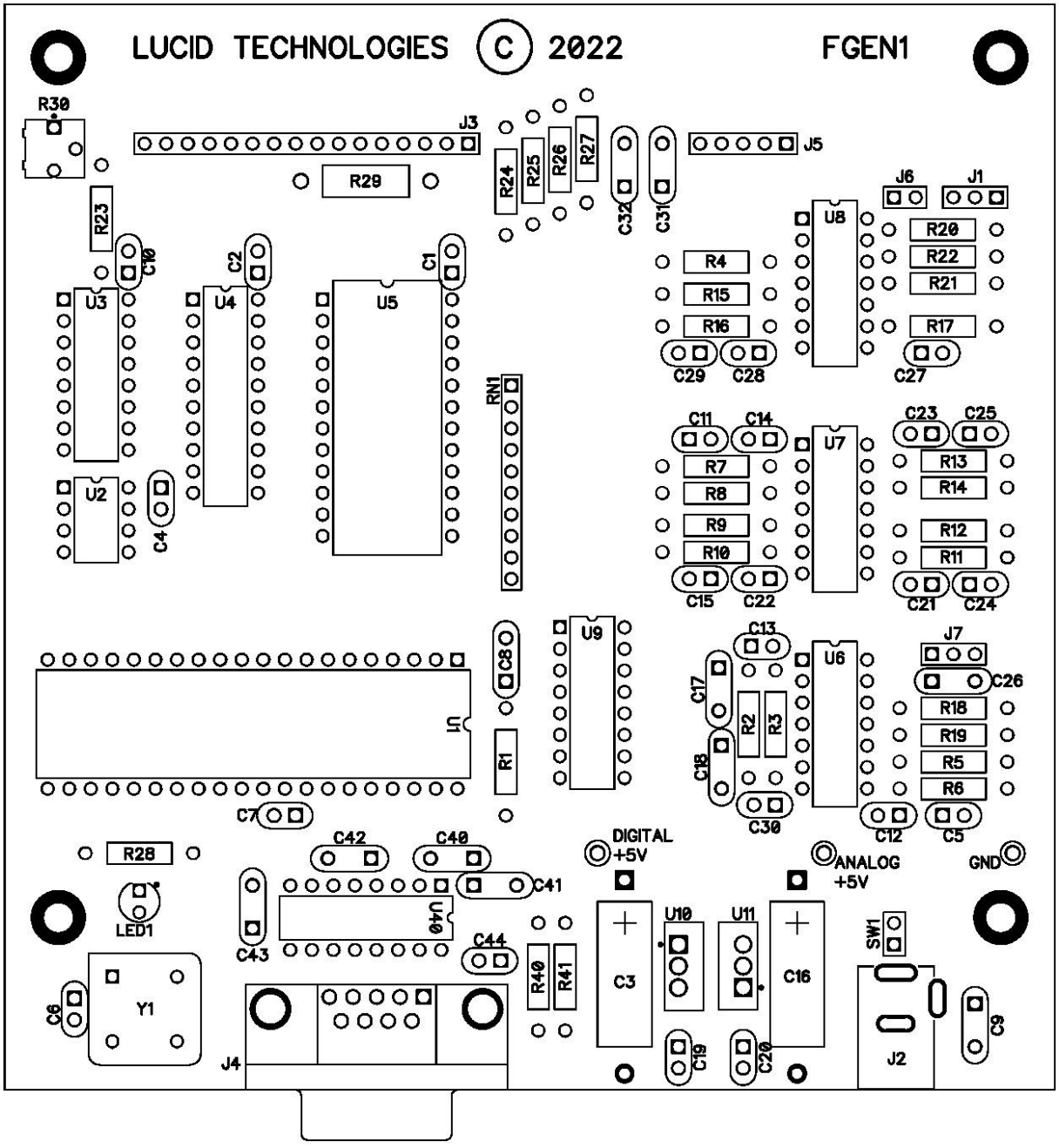


Figure H1. FGEN printed circuit board layout.

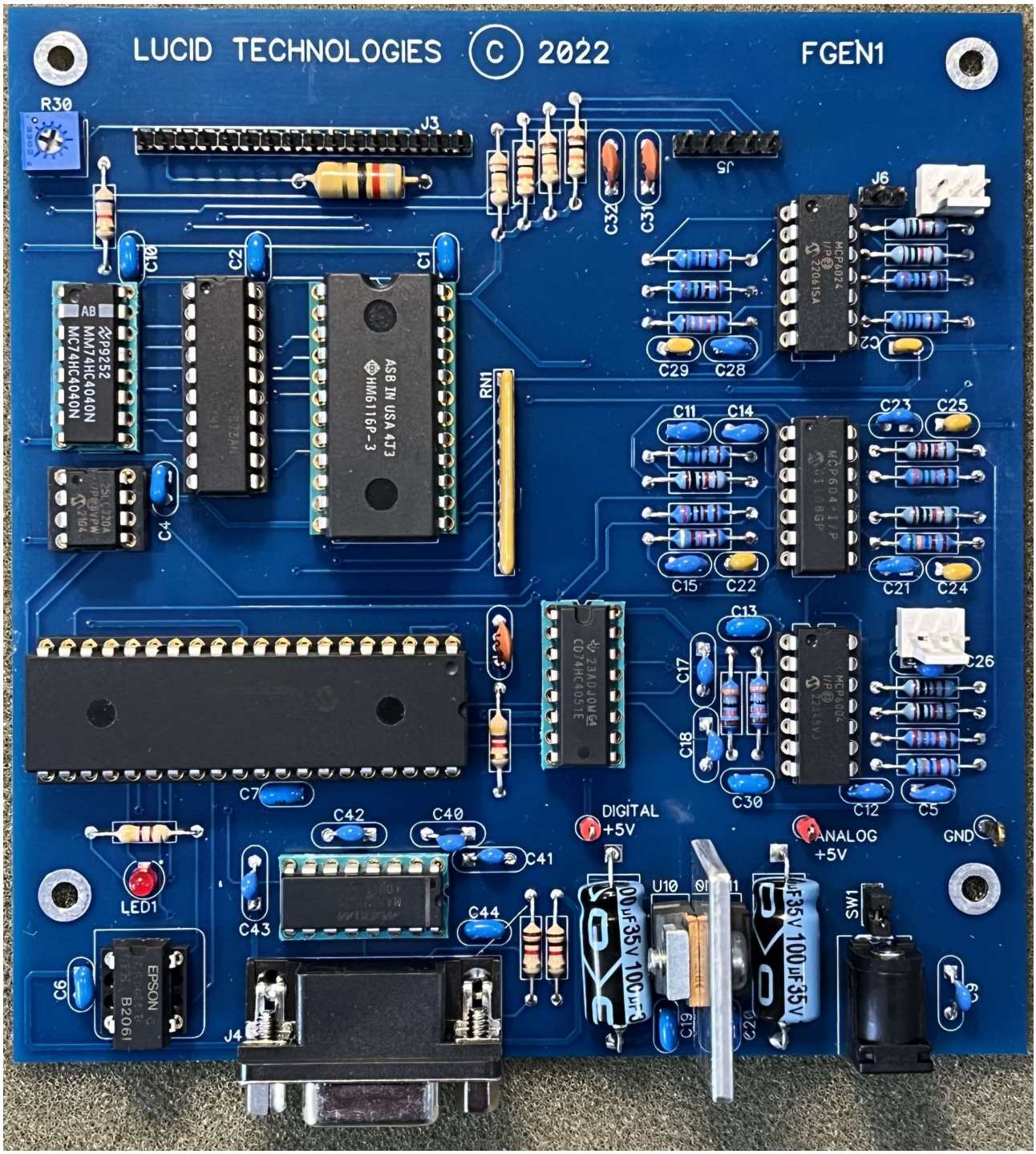
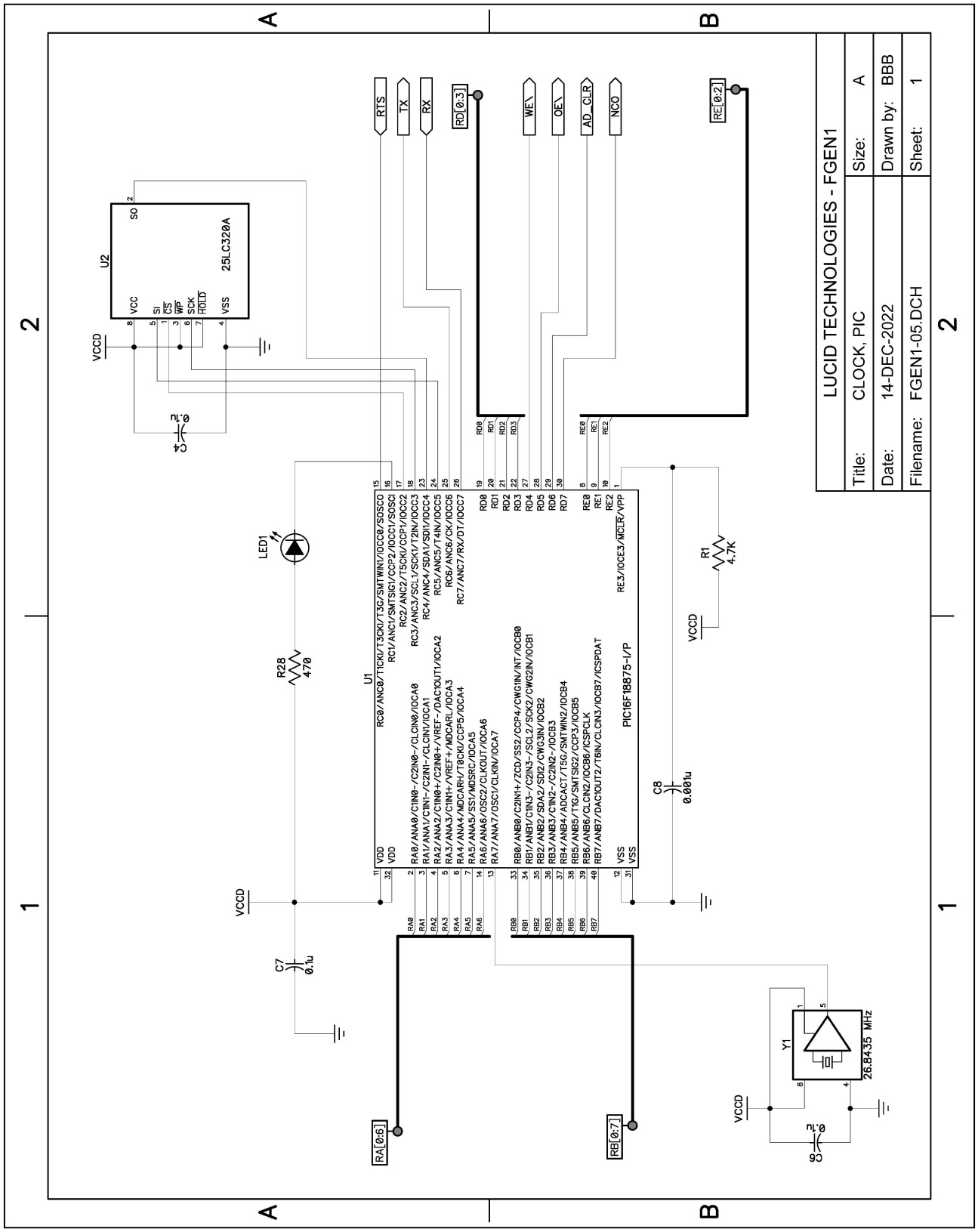
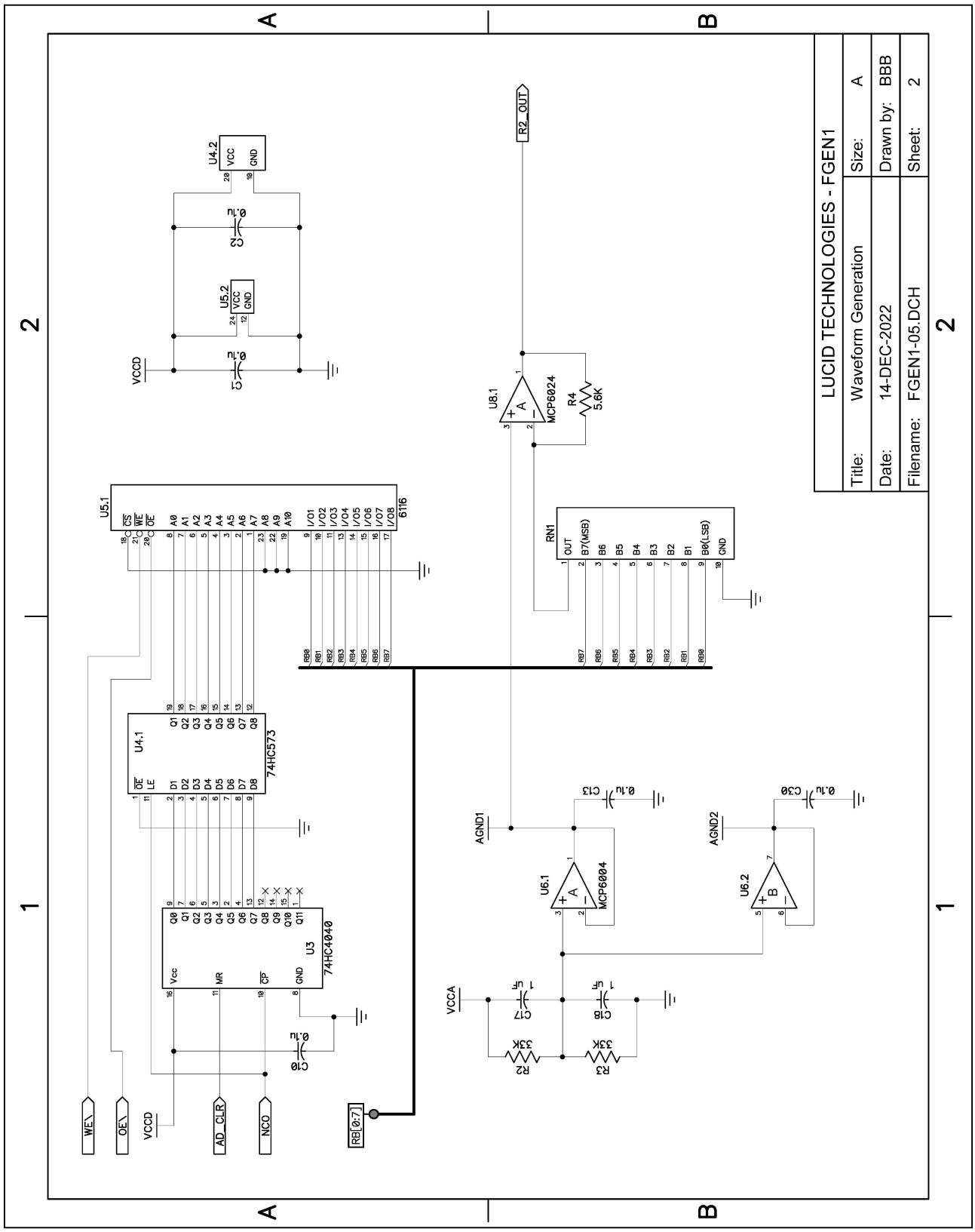
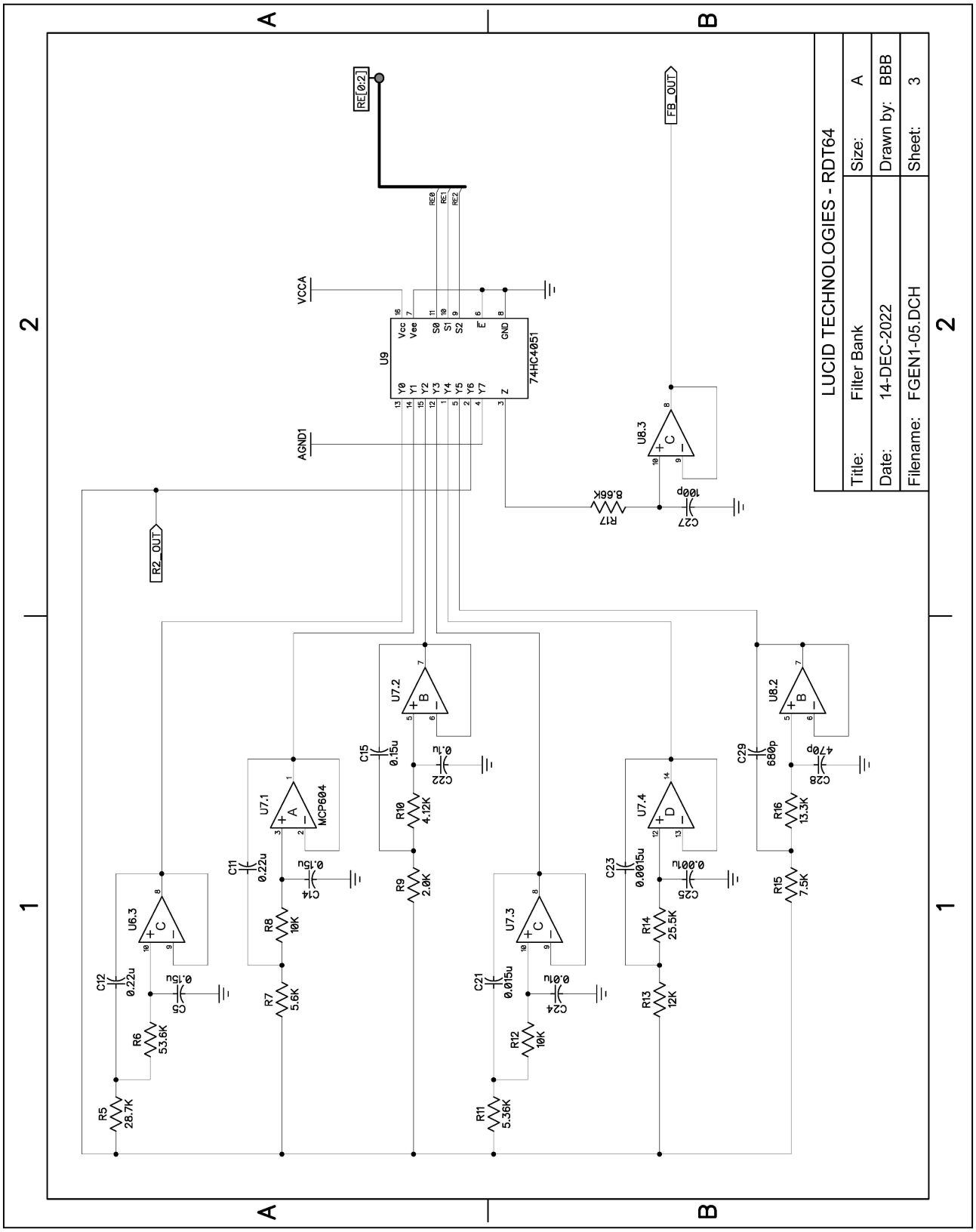


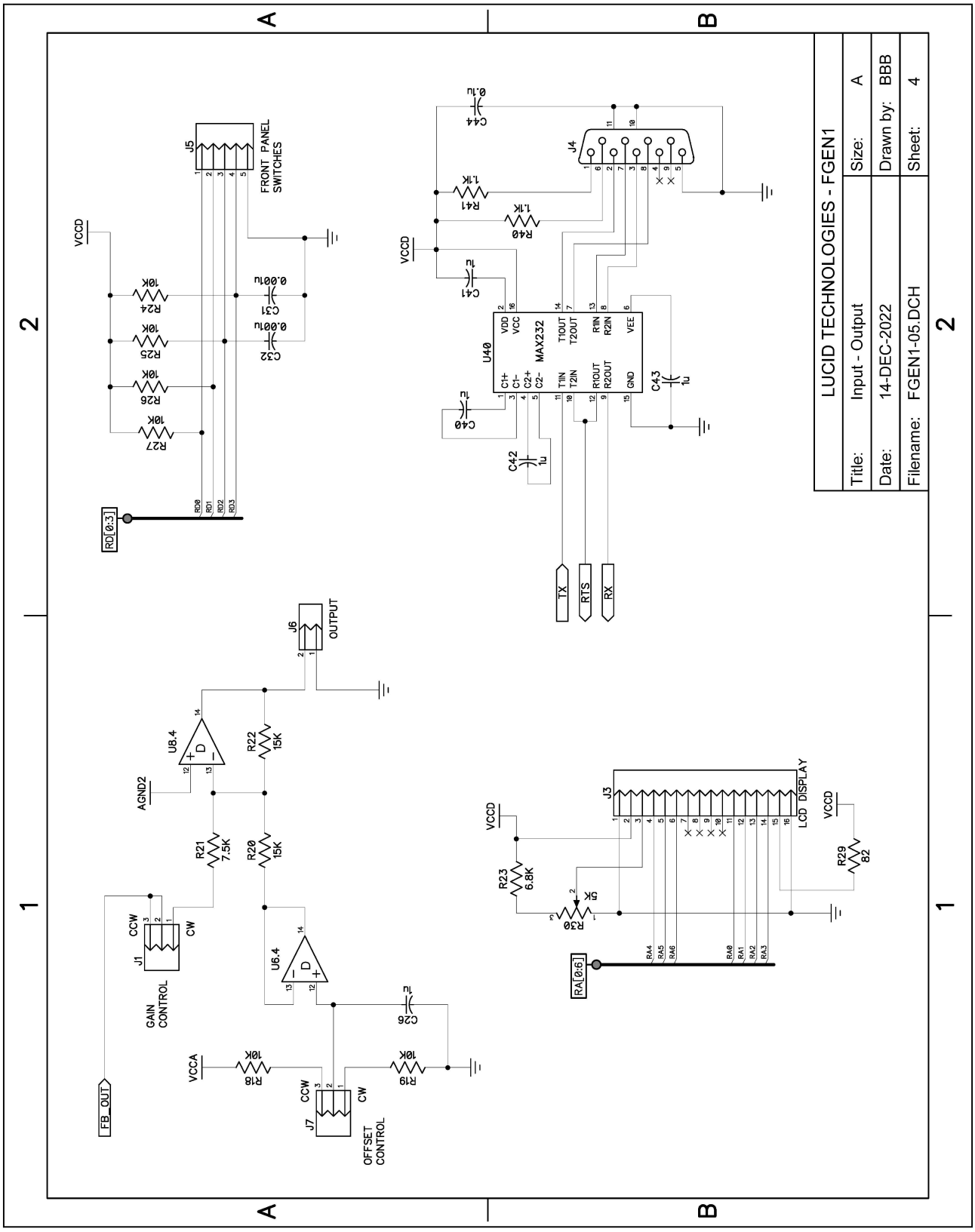
Figure H2. Assembled FGEN printed circuit board.

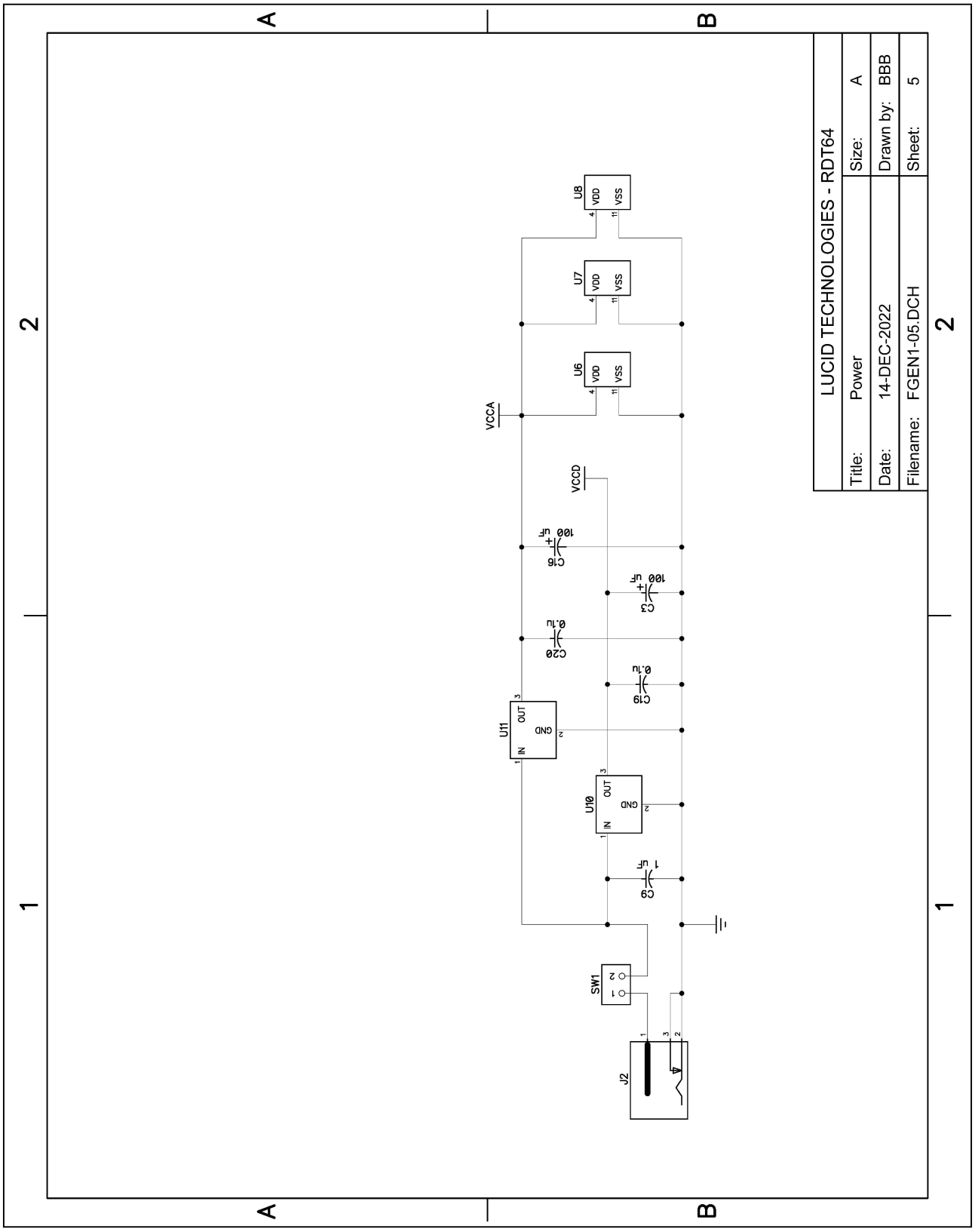
APPENDIX I


LUCID TECHNOLOGIES - FGEN1
Title: CLOCK, PIC
Size: A
Date: 14-DEC-2022
Drawn by: BBB
Filename: FGEN1-05.DCH
Sheet: 1
U1
PIC16F18875-I/P
U2
25LC320A
Y1
26.8435 MHz
LED1
R28
470
R1
4.7K
C7
0.1u
C8
0.001u
C4
0.1u
C6
0.1u
VCCD
RTS
TX
RX
RD[0:3]
WE\
OE\
AD_CLR
NCO
RE[0:2]
RA[0:6]
RB[0:7]


LUCID TECHNOLOGIES - FGEN1
Title: Waveform Generation
Size: A
Date: 14-DEC-2022
Drawn by: BBB
Filename: FGEN1-05.DCH
Sheet: 2
U4.2
VCC
GND
C2
0.1u
U5.2
VCC
GND
C1
0.1u
VCCD
U5.1
6116
CS
WE
OE
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
I/O8
RB0
RB1
RB2
RB3
RB4
RB5
RB6
RB7
U4.1
74HC573
OE
LE
D1
D2
D3
D4
D5
D6
D7
D8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
U3
74HC4040
Vcc
MR
CP
GND
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
C16
0.1u
WE\
OE\
VCCD
AD_CLR
NCO
RB[0:7]
R2_OUT
U8.1
MCP6024
R4
5.6K
RN1
OUT
B7(MSB)
B6
B5
B4
B3
B2
B1
B0(LSB)
GND
AGND1
U6.1
MCP6004
C13
0.1u
AGND2
U6.2
C30
0.1u
VCCA
C17
1uF
C18
1uF
R2
33K
R3
33K


LUCID TECHNOLOGIES - RDT64
Title: Filter Bank
Size: A
Date: 14-DEC-2022
Drawn by: BBB
Filename: FGEN1-05.DCH
Sheet: 3
RE[0:2]
FB_OUT
R2_OUT
VCCA
AGND1
U9
74HC4051
U8.3
R17 8.66K
C27 100p
U7.1
MCP604
U7.2
U7.3
U7.4
U8.2
U6.3
C11 0.22u
C14 0.15u
C15 0.15u
C22 0.1u
C12 0.22u
C5 0.15u
C21 0.015u
C24 0.01u
C23 0.0015u
C25 0.001u
C29 680p
C28 470p
R5 28.7K
R6 53.6K
R7 5.6K
R8 10K
R9 2.0K
R10 4.12K
R11 5.36K
R12 10K
R13 12K
R14 25.5K
R15 7.5K
R16 13.3K


LUCID TECHNOLOGIES - FGEN1
Title: Input - Output
Size: A
Date: 14-DEC-2022
Drawn by: BBB
Filename: FGEN1-05.DCH
Sheet: 4
J5
FRONT PANEL SWITCHES
J4
J6
OUTPUT
J3
LCD DISPLAY
J1
GAIN CONTROL
J7
OFFSET CONTROL
U40
MAX232
U8.4
U6.4
VCCD
VCCA
AGND2
RD[0:3]
RA[0:6]
FB_OUT
TX
RTS
RX
R20 15K
R21 7.5K
R22 15K
R23 6.8K
R24 10K
R25 10K
R26 10K
R27 10K
R29 82
R40 1.1K
R41 1.1K
C41 1u
C42 1u
C43 1u
C44 0.1u
C51 0.001u
C52 0.001u
C26 1u


LUCID TECHNOLOGIES - RDT64
Title: Power
Size: A
Date: 14-DEC-2022
Drawn by: BBB
Filename: FGEN1-05.DCH
Sheet: 5
A
B
1
2
U8
U7
U6
VCCA
VCCD
C16
100 uF
C3
100 uF
C20
0.1u
C19
0.1u
U11
U10
C9
1 uF
SW1
J2